8-Channel DAS with 16-Bit、1 MSPS、Bipolar Input、Simultaneous Sampling ADC

1 Features

- GD30AD3380-I10: 16-bit, 1 MSPS ADC
- GD30AD3380-I05: 16-bit, 500 KSPS ADC
- 5 V single analog supply
- VDRIVE supply voltage:
  - GD30AD3380-I10: 1.71 V to 3.6 V
  - GD30AD3380-I05: 1.71 V to 5 V
- Selectable analog input range per channel
  - GD30AD3380-I10 true bipolar hardware Mode: ±10 V, ±5 V
  - GD30AD3380-I05 true bipolar hardware Mode: ±10 V , ±5 V
  - GD30AD3380-I10 true bipolar software Mode: ±12.5 V, ±10 V, ±5 V and ±2.5 V
- with 1 MΩ analog input impedance
- Flexible digital filter for oversampling application
- Flexible paraller/serial communication interface
- ±25 V input clamp protection, 8 kV ESD
- Operating temperature range: −40 °C to +125 °C

2 Application

- Power line monitoring
- Protection relay
- Multiphase Motor Control
- Instrumentation and control systems
- Data Acquisition System

3 Description

The GD30AD3380 is a 16-bit, synchronous sampling, analog-to-digital conversion data acquisition system (DAS) with 8 channels, each with built-in analog input clamp protection, programmable gain amplifier (PGA), low-pass filter and 16-bit successive approximation register (SAR) analog-to-digital converter (ADC). The GD30AD3380 also has built-in flexible digital filters, low-drift 2.5V precision reference voltage source and reference voltage buffer (for driving ADC) and flexible parallel and serial interfaces.

The GD30AD3380 operates from a single 5 V supply and supports ±12.5 V , ±10 V , ±5 V , and ±2.5 V true bipolar input ranges when all channels are sampled at a throughput rate of 1 MSPS (GD30AD3380-I10). Input clamp protection withstands voltages up to ±25 V. The GD30AD3380 has a 1 MΩ analog input impedance, and the bipolar zero code is less than 100 LSB when the input signal is disconnected and pulled to ground through a 10 kΩ external resistor . Single-supply operation, on-chip filtering, and high input impedance eliminate the need for an external driver op amp (requires a bipolar supply). For applications with lower throughput rates, the GD30AD3380's flexible digital filter can be used to improve noise performance.

In hardware mode, GD30AD3380 is fully compatible with a mainstream model. GD30AD3380-I10 in software mode, the following advanced features can be used:

- Added ±12.5 V , ±2.5 V analog input range, selectable for each channel
- High bandwidth mode (200 kHz) , selectable per channel
- Additional oversampling (OS) options, up to OS×256
- System gain, system offset, and system phase calibration for each channel

- Analog Input Open Detector
- Diagnostic Multiplexer
- Monitoring functions (Serial Peripheral Interface (SPI) invalid read / write, cyclic redundancy check (CRC), overvoltage and undervoltage events, busy blocking monitoring, and reset detection)

Note that throughout this data sheet, multifunction pins, such as the RD/SCLK pin, are referenced either by the full pin name or by a single function of the pin; for example, the SCLK pin means only that function is relevant.

Additionally, the GD30AD3380-I05 only supports hardware mode, and all software mode-related features and functions that require configuration of registers are not supported.

Device Information [1]

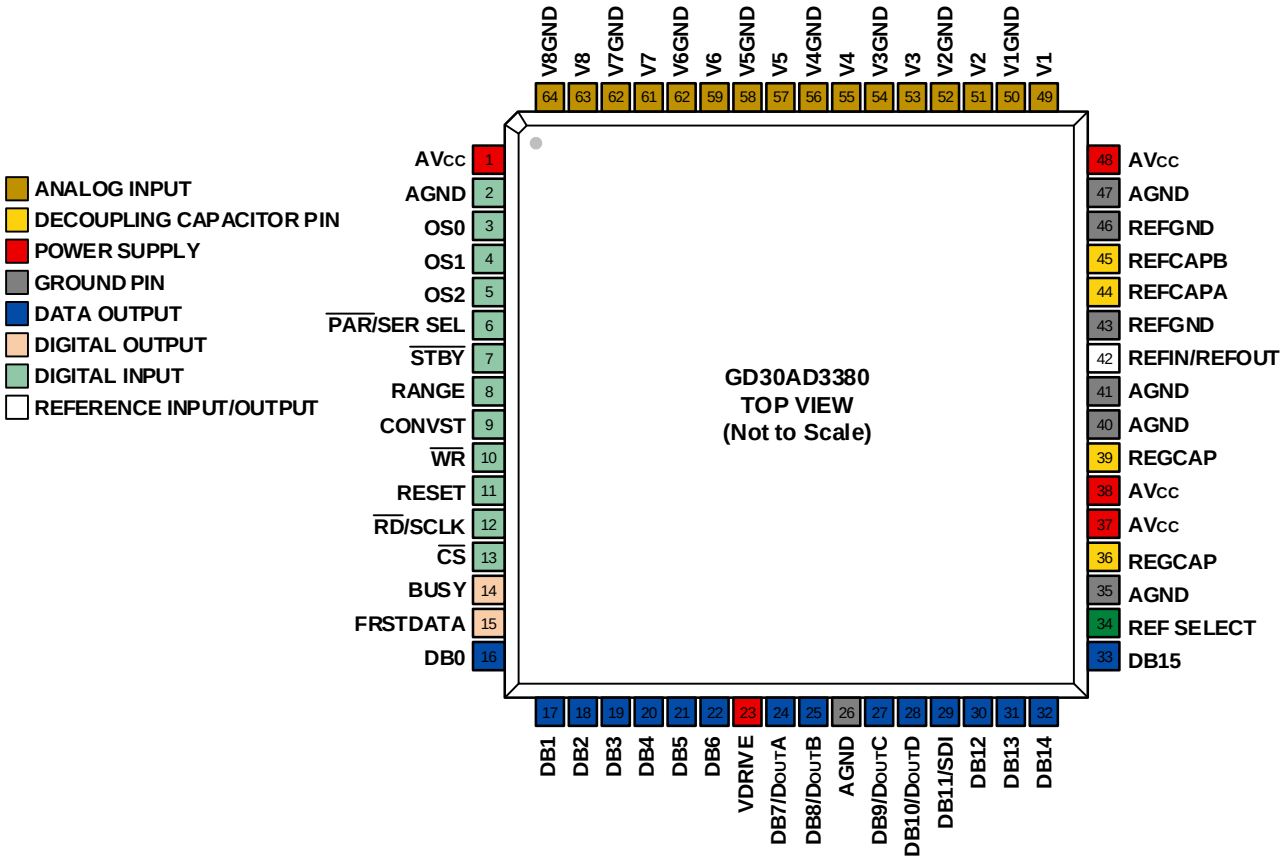
PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AD3380	LQFP 64	10.00 mm × 10.00 mm

1. For packaging details, please refer to *Packaging information* section .

Table of contents

4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PINS		TYPE [1]	FUNCTION
NAME	NUM		
AVCC	1, 37, 38, 48	P	Analog supply voltage, 4.75 V to 5.25 V. This is the supply voltage for the internal front-end amplifier and ADC core. Decouple these supply pins to AGND.
AGND	2, 26, 35, 40, 41, 47	P	Analog ground. These pins are the ground reference points for all analog circuits on the GD30AD3380. All analog input signals and external reference signals must be referenced to these pins. All six AGND pins must be connected to the system's AGND plane.
OS0 to OS2	3 to 5	DI	Oversampling mode pin. These inputs select the oversampling rate or enable software mode (see Table 4 for oversampling pin decoding). See the *Digital Filter* section for more information on the oversampling modes of operation.
$\overline{\text{PAR}}$ / SER SEL	6	DI	Parallel/Serial Interface Select Input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. See the *Digital Interface* section for more information on each available interface.
$\overline{\text{STBY}}$	7	DI	Standby mode input. In hardware mode, this pin, together with the RANGE pin, places the GD30AD3380 into one of two power-saving modes: standby mode or shutdown mode. In software mode, this pin is ignored. Therefore, it is recommended to connect this pin to a logic high level. For more information on hardware mode and software mode, see the *Power-Saving Mode* section.
RANGE	8	DI	Analog Input Range Select Input. In hardware mode, this pin determines the input range of the analog input channel (see Table 1). If the STBY pin is at logic low, this pin determines the power-saving mode (see Table 6). In software mode, the RANGE pin is ignored. However, this pin must be tied high or low.
CONVST	9	DI	Conversion start input. When the CONVST pin transitions from low to high, the analog inputs are sampled on all eight SAR ADCs. In software mode, this pin can be configured as an external oversampling clock. Providing a low jitter external clock improves SNR performance at large oversampling ratios. See the *External Oversampling Clock* section for more details.
$\overline{\text{WR}}$	10	DI	Digital input. In GD30AD3380-I10 hardware mode, this pin has no function. Therefore, it can be tied high, low, or shorted to CONVST. In GD30AD3380-I10 software mode, this pin is an active low write pin used to write registers through the parallel interface. For more information, see the *Parallel Interface* section.
RESET	11	DI	Reset input, high level is valid. Full reset and partial reset options are available. The type of reset is determined by the length of the reset pulse. It is recommended that the device receive a full reset pulse after power-up. See the Reset Functionality section for details.
$\overline{\text{RD}}$/SCLK	12	DI	Parallel data read control input (RD) when the parallel interface is selected. Serial clock input (SCLK) when a serial interface is selected. See the *Digital Interface* section for more information.
$\overline{\text{CS}}$	13	DI	Chip select. For both the serial and parallel interfaces, this pin is an active low chip select input for ADC data reading or register data reading and writing. See the Digital Interface section for more information.
BUSY	14	DO	Output busy. This pin goes logic high with the rising edge of CONVST. The BUSY output remains high until the conversion process is complete for all channels.
FRSTDATA	15	DO	First data output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel interface (see Figure 2) or the serial interface (see Figure 5). See the Digital Interface section for more information.

PINS		TYPE [1]	FUNCTION
NAME	NUM		
DB0 to DB6	16 to 22	DO/DI	Parallel output/input data bits. When using the parallel interface, these pins act as three-state parallel digital input and output pins (see the *Parallel Interface* section). When using the serial interface, these pins should be connected to AGND.
VDRIVE	twenty three	P	Logic Power Input. The supply voltage at this pin (1.71 V to 3.6 V) determines the operating voltage of the logic interface. The nominal supply at this pin is the same as the supply for the host interface, that is, the digital signal processing (DSP) and field programmable gate array (FPGA).
DB7/D_{OUT}A	twenty four	DO/DI	Parallel Output/Input Data Bit 7 (DB7)/Serial Interface Data Output Pin (D_{OUT}A). When using the parallel interface, this pin functions as a three-state parallel digital input/output pin. When using the serial interface, this pin functions as D_{OUT}A. See Table 13 and Table 14.
DB8/D_{OUT}B	25	DO/DI	Parallel Output/Input Data Bit 8 (DB8)/Serial Interface Data Output Pin (D_{OUT}B). When using the parallel interface, this pin functions as a three-state parallel digital input/output pin. When using the serial interface, this pin functions as D_{OUT}B. See Table 13 and Table 14.
DB9/D_{OUT}C	27	DO/DI	Parallel Output/Input Data Bit 9 (DB9)/Serial Interface Data Output Pin (D_{OUT}C). When using the parallel interface, this pin functions as a three-state parallel digital input/output pin. When using the serial interface, if in software mode and using the four data output lines option, this pin functions as D_{OUT}C. See Table 13 and Table 14.
DB10/D_{OUT}D	28	DO/DI	Parallel Output/Input Data Bit 10 (DB10)/Serial Interface Data Output Pin (D_{OUT}D). When using the parallel interface, this pin functions as a three-state parallel digital input/output pin. When using the serial interface, if in software mode and using the four data output lines option, this pin functions as D_{OUT}D. See Table 13 and Table 14.
DB11/SDI	29	DO/DI	Parallel output/input data bit DB11/serial data input. When using the parallel interface, this pin functions as a three-state parallel digital input/output pin. When using the serial interface in software mode, this pin functions as a serial data input. For more information on the operating modes, see Table 13 and Table 14.
DB12 to DB15	30 to 33	DO/DI	Parallel output/input data bits DB15 to DB12. When using the parallel interface, these pins act as three-state parallel digital input and output pins (see the *Parallel Interface* section). When using the serial interface, these pins should be connected to AGND.
REF SELECT	34	DI	Internal/external reference voltage selection logic input. If this pin is set to logic high, the internal reference mode is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference must be applied to the REFIN/REFOUT pin.
REGCAP	36, 39	P	Decoupling capacitor pin, Voltage outputs for the 1.9 V internal regulator, the analog low dropout (ALDO), and the digital low dropout (DLDO) regulators. These output pins must be individually decoupled to AGND using 1 µF capacitors.
REFIN/ REFOUT	42	REF	Reference voltage input (REFIN)/reference voltage output (REFOUT). The internal 2.5 V reference can be made available for external use through the REFOUT pin while setting the REF SELECT pin to logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to logic low, in which case an external 2.5 V reference must be applied to this input (REFIN). For both the internal and external reference options, a 100 nF capacitor must be applied from the REFIN pin to ground (close to the REFGND pin). See the *Reference* section for details.
REFGND	43, 46	REF	Reference Voltage Ground Pin. These pins must be connected to AGND.
REFCAPA, REFCAPB	44, 45	REF	Reference Voltage Buffered Output Force/Sense Pin. These pins must be tied together and decoupled to AGND via low ESR (effective series resistance), 10 µF ceramic capacitors. The voltage on these pins is typically 4.4 V.

PINS		TYPE [1]	FUNCTION
NAME	NUM		
V1	49	AI	Channel 1 Positive Analog Input Pin.
V1GND	50	AI GND	Channel 1 negative analog input pin.
V2	51	AI	Channel 2 Positive Analog Input Pin.
V2GND	52	AI GND	Channel 2 Negative Analog Input Pin.
V3	53	AI	Channel 3 Positive Analog Input Pin.
V3GND	54	AI GND	Channel 3 Negative Analog Input Pin.
V4	55	AI	Channel 4 Positive Analog Input Pin.
V4GND	56	AI GND	Channel 4 Negative Analog Input Pin.
V5	57	AI	Channel 5 Positive Analog Input Pin.
V5GND	58	AI GND	Channel 5 Negative Analog Input Pin.
V6	59	AI	Channel 6 Positive Analog Input Pin.
V6GND	60	AI GND	Channel 6 Negative Analog Input Pin.
V7	61	AI	Channel 7 Positive Analog Input Pin.
V7GND	62	AI GND	Channel 7 Negative Analog Input Pin.
V8	63	AI	Channel 8 Positive Analog Input Pin.
V8GND	64	AI GND	Channel 8 Negative Analog Input Pin.

1. P stands for power supply, DI stands for digital input, DO stands for digital output, REF stands for reference voltage input / output, AI stands for analog input, and GND stands for ground.

5 Parameter information

5.1 Absolute Maximum Ratings

Unless otherwise noted, T_A = 25°C.

PARAMETER	RATING
AV_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AVCC + 0.3 V
Analog input voltage to AGND[1]	±25 V
Digital input voltage to AGND	−0.3 V to VDRIVE + 0.3 V
Digital output voltage to AGND	−0.3 V to VDRIVE + 0.3 V
REFIN to AGND	−0.3 V to AVCC + 0.3 V
Input current into any pin except supply pins1	±10 mA
Operating temperature range	−40°C to +125°C
Storage temperature range	−65°C to +150°C
Junction temperature	150°C
Lead-tin soldering temperature	
Reflow (10 seconds to 30 seconds)	240 (+0)°C
Lead-free reflow temperature	260 (+0)°C
Electrostatic Discharge (ESD)	
All pins except analog input	3.5 kV
Analog input pins only	7 kV

1. Transient currents below 100 mA will not cause silicon-controlled rectifier (SCR) latch-up.
2. Note that exposure to conditions equal to or exceeding the absolute maximum ratings listed above may cause permanent damage to the product. These are maximum ratings only and do not imply that the device will operate normally under these conditions or any other conditions beyond those shown in the operational section of this technical specification. Extended exposure to conditions exceeding the maximum ratings may affect product reliability.

5.2 Thermal resistance

Thermal performance is directly related to the printed circuit board (PCB) design and the operating environment. PCB heat dissipation design must be treated with caution.
θ_{JA} is the junction-to-ambient thermal resistance under natural convection, measured in a 1 cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

PACKAGE TYPE	θ_{JA}[1]	θ_{JC}[1]	UNIT
LQFP-64	40	7	°C/W

1. Simulation data based on JEDEC 2S2P thermal test PCB in JEDEC natural convection environment.

5.3 GD30AD3380-I10 Electrical Characteristic

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V , logic supply voltage (V_{DRIVE}) = 1.71 V to 3.6 V , sampling frequency (f_{SAMPLE}) = 1 MSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Dynamic performance	Input frequency (f_{IN}) = 1 kHz sine wave unless otherwise noted				
Signal-to-Noise Ratio (SNR)[1] Low Bandwidth Mode	No OS, ±12.5 V range	87	90		dB
	No OS, ±10 V range	87	90		dB
	No OS, ±5 V range	86	88.5		dB

GD30AD3380-I10 Electrical Characteristic(Continued)

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V , logic supply voltage (V_{DRIVE}) = 1.71 V to 3.6 V , sampling frequency (f_{SAMPLE}) = 1 MSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
	No OS, ±2.5 V range	83	86		dB
	OSR = 16×，±12.5 V range	93	96		dB
	OSR = 16×，±10 V range	92	95.5		dB
	OSR = 16×，±5 V range	91	94		dB
	OSR = 16×，±2.5 V range	89	92		dB
Signal-to-Noise Ratio (SNR) [1] High Bandwidth Mode	No OS，±12.5 V range		87.5		dB
	No OS，±10 V range		88		dB
	No OS，±5 V range		84		dB
	No OS，±2.5 V range		81.5		dB
Total Harmonic Distortion (THD)--Low bandwidth mode	All input ranges		−103	−94	dB
SNR--Low bandwidth mode	No OS，±12.5 V range	87	90		dB
	No OS，±10 V range	87	90		dB
	No OS，±5 V range	86	89		dB
	No OS，±2.5 V range	83	86		dB
	OSR = 16×，±12.5 V range	92	95		dB
	OSR = 16×，±10 V range	91	94		dB
	OSR = 16×，±5 V range	90	93.5		dB
	OSR = 16×，±2.5 V range	88	91.5		dB
SNR--High Bandwidth Mode	No OS，±12.5 V range		87		dB
	No OS，±10 V range		87		dB
	No OS，±5 V range		83		dB
	No OS，±2.5 V range		81		dB
Spurious Free Dynamic Range (SFDR)			−104		dB
Channel-to-channel isolation	f_{IN} up to 160 kHz for unselected channels		−110		dB
Analog Input Filter					
Full Power Bandwidth--Low Bandwidth Mode	−3 dB		25		kHz
	−0.1 dB		3.9		kHz
Full Power Bandwidth--High Bandwidth Mode	−3 dB		200		kHz
	−0.1 dB		25		kHz
Phase Delay--Low Bandwidth Mode	±12.5 V, ±10 V range		6.9		µs
	±5 V range		6.7		µs
	±2.5 V range		6		µs

GD30AD3380-I10 Electrical Characteristic(Continued)

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V , logic supply voltage (V_{DRIVE}) = 1.71 V to 3.6 V , sampling frequency (f_{SAMPLE}) = 1 MSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Phase Delay--High Bandwidth Mode	±12.5 V, ±10 V range		0.3		μs
	±5 V range		0.1		μs
	±2.5 V range		−0.6		μs
Phase Delay Matching – Low Bandwidth Mode				200	ns
Phase Delay Matching – High Bandwidth Mode				30	ns
DC accuracy					
Resolution	No missing codes	16			位
Differential Nonlinearity (DNL)			±0.6	±0.99	LSB[2]
Integral Nonlinearity (INL)	f_{SAMPLE} = 1 MSPS		±1	±2.5	LSB[2]
Total Unadjusted Error (TUE)	Internal voltage reference		±16		LSB
Positive and negative full scale (FS) error [3]	External voltage reference		±8	±50	LSB
	Internal voltage reference		±8		LSB
Positive and negative full scale (FS) error drift	External voltage reference		±4		ppm/°C
	Internal voltage reference		±8		ppm/°C
Positive and negative FS error matching			12	60	LSB
Bipolar Zero Code Error			±3	±12	LSB[2]
Bipolar Zero Code Error Drift			±0.6	±2	ppm/°C
Bipolar Zero Code Error Matching			6	24	LSB[2]
Analog Input					
Input voltage range	Vx − VxGND				
	±12.5 V range	−12.5		+12.5	V
	±10 V range	−10		+10	V
	±5 V range	−5		+5	V
	±2.5 V range	−2.5		+2.5	V
Input voltage range	VxGND − AGND				
	±12.5 V range	−1		+1.6	V
	±10 V range	−0.7		+1.9	V
	±5 V range	−0.1		+2.7	V
	±2.5 V range	−0.1		+3.1	V
Analog input current			8		μA
Input Capacitor(C)[4]			5		pF
Input impedance (R)[5]		1			MΩ
Reference voltage input/output					
Reference input voltage	REF SELECT=0，External voltage reference	2.475	2.5	2.525	V

GD30AD3380-I10 Electrical Characteristic(Continued)

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V , logic supply voltage (V_{DRIVE}) = 1.71 V to 3.6 V , sampling frequency (f_{SAMPLE}) = 1 MSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
DC leakage current				±0.1	μA
Input Capacitor[4]			7.5		pF
Reference output voltage	REF SELECT=1，Internal voltage reference, T_A = 25°C	2.495	2.5	2.505	V
Reference source temperature coefficient			±10		ppm/°C
ADC reference voltage	REFCAPA（PIN 44）和 REFCAPB（PIN 45）	4.086	4.096	4.106	V
Logic Input					
Input High Voltage (V_{INH})		0.7×V_{DRIVE}			V
Input Low Voltage (V_{INL})				0.3×V_{DRIVE}	V
Input Current (I_{IN})				±1	μA
Input Capacitor [4]			5		pF
Logic Output					
Output high voltage (V_{OH})	Source current (I_{SOURCE}) = 100 μA	V_{DRIVE}−0.2			V
Output low voltage (V_{OL})	Sink current (I_{SINK}) = 100 μA			0.2	V
Floating state leakage current			±1	±20	μA
Output capacitor[6]			5		pF
Output Encoding	Two's complement				N/A[6]
Conversion rate					
Conversion time			0.54		μs
Collection time			0.46		μs
Throughput rate	Per channel			1	MSPS
Power Requirements					
AV_{CC}		4.75	5	5.25	V
V_{DRIVE}		1.71	3.3	3.6	V
REGCAP		1.875		1.93	V
AV_{CC} Current (I_{AVCC})					
Normal mode (static)			10.6		mA
Normal mode (working state)	f_{SAMPLE} = 1 MSPS		25.5		mA
	f_{SAMPLE} = 10 KSPS		11.4		mA
Standby			7.2		mA
Shutdown Mode			0.6		μA
I_{DRIVE}					
Normal mode (static)			0.2		μA
Normal mode (working state)	f_{SAMPLE} = 1 MSPS		1.6		mA
	f_{SAMPLE} = 10 KSPS		30		μA
Standby			0.16		μA

GD30AD3380-I10 Electrical Characteristic(Continued)

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V , logic supply voltage (V_{DRIVE}) = 1.71 V to 3.6 V , sampling frequency (f_{SAMPLE}) = 1 MSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Shutdown Mode			0.1		μA
Power consumption					
Normal mode (static)			53		mW
Normal mode (working state)	f_{SAMPLE} = 1 MSPS		133		mW
	f_{SAMPLE} = 10 KSPS		57		mW
Standby			36		mW
Shutdown Mode			3.5		μW

1. No OS means no oversampling is applied.
2. LSB stands for least significant bit. For ±2.5 V input range, 1 LSB = 76.293 μV. For ±5 V input range, 1 LSB = 152.58 μV. For ±10 V input range, 1 LSB = 305.175 μV.
3. These specifications include full temperature variation as well as the contribution from the internal reference and reference buffer.
4. Not production tested. Samples are tested during initial release to ensure compliance with standards.
5. N/A means not applicable.

5.4 GD30AD3380-I05 Electrical Characteristic

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25V , logic supply voltage (V_{DRIVE}) = 1.71 V to 5 V , sampling frequency (f_{SAMPLE}) = 500 KSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Dynamic performance	Input frequency (f_{IN}) = 1 kHz sine wave unless otherwise noted				
Signal-to-Noise Ratio (SNR)[1] Low Bandwidth Mode	No OS，±10 V range	87	90		dB
	No OS，±5 V range	86	89		dB
	OSR = 16×，±10 V range	92	95.5		dB
	OSR = 16×，±5 V range	91	94		dB
Total Harmonic Distortion (THD)			−103	-94	dB
Signal-to-Noise Ratio (SNR)	No OS，±12.5 V range	87	90		dB
	No OS，±10 V range	87	90		dB
Spurious Free Dynamic Range (SFDR)			−104		dB
Channel-to-channel isolation	f_{IN} up to 20 kHz for unselected channels		−110		dB
Analog Input Filter					
Full Power Bandwidth--Low Bandwidth Mode	−3 dB, ±10 V range		25		kHz
	−3 dB, ±5 V range		25		kHz
	−0.1 dB, ±10 V range		3.9		kHz
	−0.1 dB, ±5 V range		3.9		kHz
Phase Delay	±10 V range		6.9		μs
	±5 V range		6.7		μs
Phase Delay Matching				200	ns
DC accuracy					

GD30AD3380-I05 Electrical Characteristic(Continued)

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V , logic supply voltage (V_{DRIVE}) = 1.71 V to 5 V , sampling frequency (f_{SAMPLE}) = 500 KSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Resolution	No missing codes	16			位
Differential Nonlinearity (DNL)			±0.6	±0.99	LSB[2]
Integral Nonlinearity (INL)	f_{SAMPLE} = 1 MSPS		±1	±2.5	LSB[2]
Total Unadjusted Error (TUE)	±10V range		±10		LSB
	±5V range		±16		LSB
Positive and negative full scale (FS) error [3]	External voltage reference		±8	±50	LSB
	Internal voltage reference		±8		LSB
Positive and negative full scale (FS) error drift	External voltage reference		±4		ppm/°C
	Internal voltage reference		±8		ppm/°C
Positive and negative FS error matching	±10V range		10	50	LSB
	±5V range		12	60	LSB
Bipolar Zero Code Error	±10V range		±1	±6	LSB[2]
	±5V range		±3	±12	LSB
Bipolar Zero Code Error Drift	±10V range		10		μV/°C
Bipolar Zero Code Error Matching	±10V range		1	12	LSB2
	±5V range		6	24	LSB
Analog Input					
Input voltage range	Vx − VxGND				
	±10 V range	−10		+10	V
	±5 V range	−5		+5	V
Input voltage range	VxGND − AGND				
	±10 V range	−0.7		+1.9	V
	±5 V range	−0.1		+2.7	V
Analog input current			8		μA
Input Capacitor(C)[4]			5		pF
Input impedance (R)[5]			1		MΩ
Reference voltage input/output					
Reference input voltage	REF SELECT=0, external reference voltage source	2.475	2.5	2.525	V
DC leakage current				±0.1	μA
Input Capacitor[4]			7.5		pF
Reference output voltage	REF SELECT=1, internal reference voltage source		2.5		V
Reference source temperature coefficient			±10		ppm/°C
ADC reference voltage					
Input High Voltage (V_{INH})		0.7×V_{DRIVE}			V

GD30AD3380-I05 Electrical Characteristic(Continued)

Unless otherwise noted, reference voltage (V_{REF}) = 2.5 V internal reference, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V , logic supply voltage (V_{DRIVE}) = 1.71 V to 5 V , sampling frequency (f_{SAMPLE}) = 500 KSPS, no oversampling, T_A = −40 °C to +125 °C, single-ended input, all input voltage ranges.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Low Voltage (V_{INL})				0.3×V_{DRIVE}	V
Input Current (I_{IN})				±2	μA
Input Capacitor [4]			5		pF
Logic Output					
Output high voltage (V_{OH})	Source current (ISOURCE) = 100 μA	V_{DRIVE}−0.2			V
Output low voltage (V_{OL})	Sink current (ISINK) = 100 μA			0.2	V
Floating state leakage current			±1	±20	μA
Output capacitor 6			5		pF
Output Encoding	Two's complement				N/A5
Conversion rate					
Conversion time			1.0		μs
Collection time			1.0		μs
Throughput rate	Per channel			500	KSPS
Power Requirements					
AVCC		4.75	5	5.25	V
VDRIVE		1.71	3.3	5.25	V
AV_{CC} Current (I_{AVCC})					
Normal mode (static)			10		mA
Normal mode (working state)	f_{SAMPLE} = 500 KSPS		22		mA
Standby			7.2		mA
Shutdown Mode			0.6		μA
I_{DRIVE}					
Normal mode (static)			30		μA
Normal mode (working state)	f_{SAMPLE} = 500 KSPS		1.7		mA
Standby			0.16		μA
Shutdown Mode			0.1		μA
Power consumption					
Normal mode (static)			50		mW
Normal mode (working state)	f_{SAMPLE} = 500 KSPS		116		mW
Standby			36		mW
Shutdown Mode			3.5		μW

1. No OS means no oversampling is applied.
2. LSB stands for least significant bit. For ±2.5 V input range, 1 LSB = 76.293 μV. For ±5 V input range, 1 LSB = 152.58 μV. For ±10 V input range, 1 LSB = 305.175 μV.
3. These specifications include full temperature variation as well as the contribution from the internal reference and reference buffer.
4. Not production tested. Samples are tested during initial release to ensure compliance with standards.
5. N/A means not applicable.

5.5 Timing Specifications

5.5.1 GD30AD3380-I10 General Timing Specifications

AV_{CC} = 4.75 V to 5.25 V , V_{DRIVE} = 1.71 V to 3.6 V , V_{REF} = 2.5 V external reference and internal reference, T_A = −40°C to +125°C, unless otherwise noted . Interface timing is tested with 20 pF load capacitance and is dependent on V_{DRIVE} and the load capacitance of the serial interface.

PARAMETER	MIN	TYP	MAX	UNIT	DESCRIBE
t_{CYCLE}	1			μs	Minimum time between consecutive CONVST rising edges (excluding oversampling mode)[1]
t_{LP_CNV}	80			ns	CONVST low level pulse width
t_{HP_CNV}	80			ns	CONVST high level pulse width
$t_{D\_CNV\_BSY}$					CONVST high level to BUSY high level delay time
			20	ns	V_{DRIVE} > 2.7 V
			25	ns	V_{DRIVE} < 2.7 V
t_{S_BSY}	0			ns	From the BUSY falling edge to $\overline{RD}$ the falling edge setup time (parallel interface) or to the $D_{OUT}X$ line providing the MSB (serial interface)
t_{D_BSY}			25	ns	The last $\overline{RD}$ falling edge (*Parallel Interface*) or the last LSB being clocked out (*Serial Interface*) to the subsequent BUSY falling edge; read during conversion
t_{CONV}	0.5		0.62	μs	Conversion time; no oversampling
	2.2		2.3	μs	2x oversampling
	4.65		4.8	μs	4x oversampling
	9.6		9.9	μs	8x oversampling
	19.4		20	μs	16x oversampling
	39.2		40.2	μs	32x oversampling
	78.7		80.8	μs	64x oversampling
	157.6		161.9	μs	128 times oversampling
	315.6		324	μs	256 times oversampling
t_{RESET}					
Partial Reset	55		2000	ns	Partial RESET high level pulse width
Complete reset	3000			ns	Full RESET high level pulse width
t_{DEVICE_SETUP}				μs	Time between RESET falling edge and first CONVST rising edge
Partial Reset	80			ns	
Complete reset	600			μs	
$t_{WAKE-UP}$					Wake-up time after standby/shutdown mode
Standby	1			μs	
Shutdown	10			ms	
$t_{POWER-UP}$	10			ms	Time between stable V_{CC} /V_{DRIVE} and RESET assertion

1. Applicable in serial mode (when all four $D_{OUT}X$ lines are selected).

5.5.2 GD30AD3380-I05 General Timing Specifications

AV_{CC} = 4.75 V to 5.25 V , V_{DRIVE} = 1.71 V to 5 V , V_{REF} = 2.5 V external reference and internal reference, T_A = −40°C to +125°C, unless otherwise noted . Interface timing is tested with 20 pF load capacitance and is dependent on V_{DRIVE} and the load capacitance of the serial interface.

PARAMETER	MIN	TYP	MAX	UNIT	DESCRIBE
t_{CYCLE}	2			μs	Minimum time between consecutive CONVST rising edges (excluding oversampling mode)[1]
t_{LP_CNV}	80			ns	CONVST low level pulse width
t_{HP_CNV}	80			ns	CONVST high level pulse width
$t_{D\_CNV\_BSY}$					CONVST high level to BUSY high level delay time
			20	ns	V_{DRIVE} > 2.7 V
			25	ns	V_{DRIVE} < 2.7 V
t_{S_BSY}	0			ns	From the BUSY falling edge to $\overline{RD}$ the falling edge setup time (parallel interface) or to the $D_{OUT}X$ line providing the MSB (serial interface)
t_{D_BSY}			25	ns	The last $\overline{RD}$ falling edge (*Parallel Interface*) or the last LSB being clocked out (*Serial Interface*) to the subsequent BUSY falling edge; read during conversion
t_{CONV}	0.9		1	μs	Conversion time; no oversampling
	2.6		2.7	μs	2x oversampling
	5		5.2	μs	4x oversampling
	10		10.3	μs	8x oversampling
	19.8		20.4	μs	16x oversampling
	39.6		40.6	μs	32x oversampling
	79.1		81.2	μs	64x oversampling
				μs	128 times oversampling
	55		2000	μs	256 times oversampling
t_{RESET}	3000				
Partial Reset				ns	Partial RESET high level pulse width
Complete reset	80			ns	Full RESET high level pulse width
t_{DEVICE_SETUP}	600			μs	Time between RESET falling edge and first CONVST rising edge
Partial Reset				ns	
Complete reset	1			μs	
$t_{WAKE-UP}$	10				Wake-up time after standby/shutdown mode
Standby	10			μs	
Shutdown	2			ms	
$t_{POWER-UP}$	80			ms	Time between stable V_{CC} /V_{DRIVE} and RESET assertion

2. Applicable in serial mode (when all four $D_{OUT}X$ lines are selected).

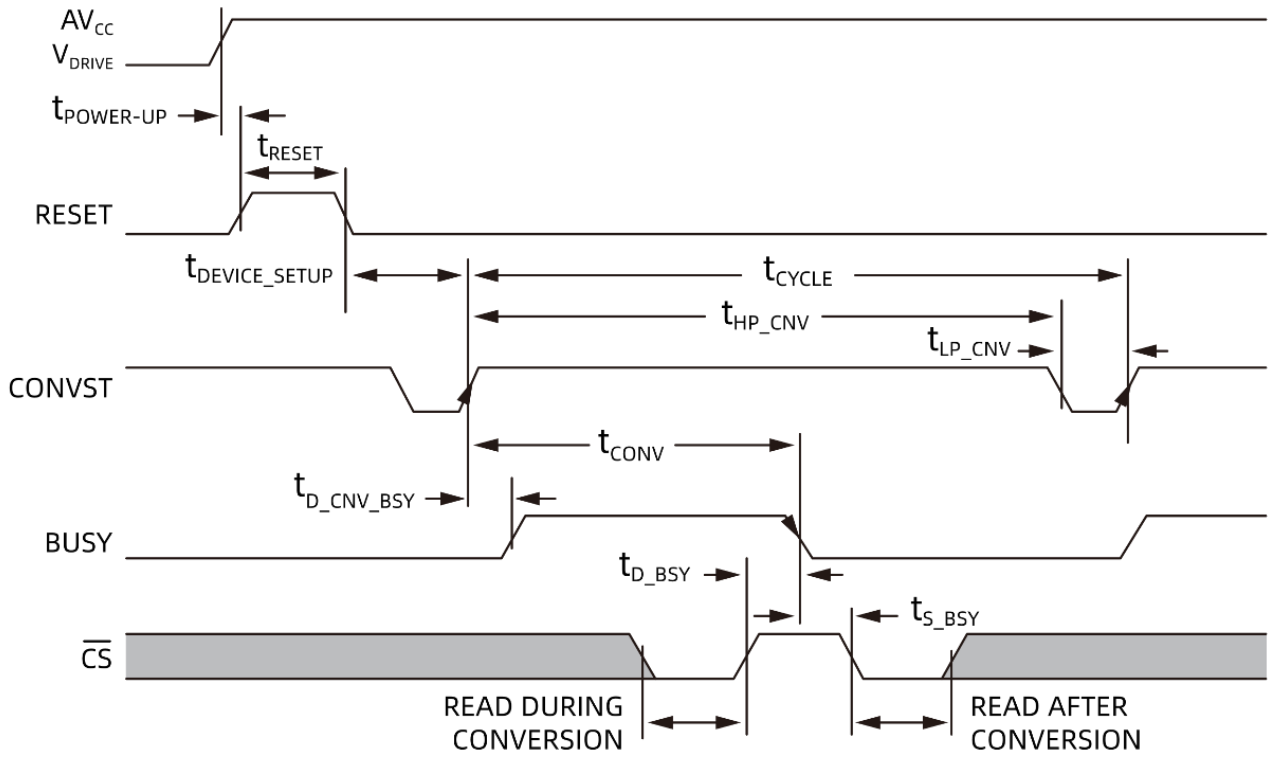


Figure 1. GD30AD3380-I10/I05 General Timing Diagram

5.5.3 Parallel Mode Timing Specifications

PARAMETER	MIN	TYP	MAX	UNIT	DESCRIBE
$t_{S\_\overline{CS}\_RD}$	0			ns	$\overline{CS}$ Falling edge to $\overline{RD}$ falling edge setup time
$t_{H\_RD\_\overline{CS}}$	0			ns	$\overline{RD}$ Rising edge to $\overline{CS}$ rising edge hold time
t_{HP_RD}	10			ns	$\overline{RD}$ High level pulse width
t_{LP_RD}	10			ns	$\overline{RD}$ Low level pulse width
$t_{HP\_\overline{CS}}$	10			ns	$\overline{CS}$ High level pulse width
$t_{D\_\overline{CS}\_DB}$			35	ns	From $\overline{CS}$ to DBx tri-state disable
$t_{H\_\overline{CS}\_DB}$	0			ns	$\overline{CS}$ to DBx hold time
$t_{D\_RD\_DB}$					$\overline{RD}$ Data access time after falling edge
			27	ns	V_{DRIVE} > 2.7 V
			37	ns	V_{DRIVE} < 2.7 V
$t_{H\_RD\_DB}$	12			ns	$\overline{RD}$ Data hold time after falling edge
$t_{DHZ\_\overline{CS}\_DB}$			40	ns	$\overline{CS}$ Rising to DBx high impedance
t_{CYC_RD}					$\overline{RD}$ Falling edge to next $\overline{RD}$ falling edge
	30			ns	V_{DRIVE} > 2.7 V
	40			ns	V_{DRIVE} < 2.7 V
$t_{D\_\overline{CS}\_FD}$			26	ns	From $\overline{CS}$ falling edge to FRSTDATA tri-state disable
$t_{D\_RD\_FDH}$			30	ns	From $\overline{RD}$ falling edge to FRSTDATA high level
$t_{D\_RD\_FDL}$			30	ns	From $\overline{RD}$ falling edge to FRSTDATA low level
t_{DHZ_FD}			28	ns	From $\overline{CS}$ rising edge to FRSTDATA tri-state enable
$t_{S\_\overline{CS}\_WR}$	0			ns	$\overline{CS}$ to $\overline{WR}$ build time
t_{HP_WR}	213			ns	$\overline{WR}$ High level pulse width
t_{LP_WR}					$\overline{WR}$ Low level pulse width
	88			ns	V_{DRIVE} > 2.7 V
	213			ns	V_{DRIVE} < 2.7 V
$t_{H\_WR\_\overline{CS}}$	0			ns	$\overline{WR}$ Keep time
$t_{S\_DB\_WR}$	5			ns	Configuration data to $\overline{WR}$ establishment time
$t_{H\_WR\_DB}$	5			ns	Configuration data to $\overline{WR}$ hold time
t_{CYC_WR}	230			ns	Configuration data setup time, $\overline{WR}$ rising edge to next $\overline{WR}$ rising edge

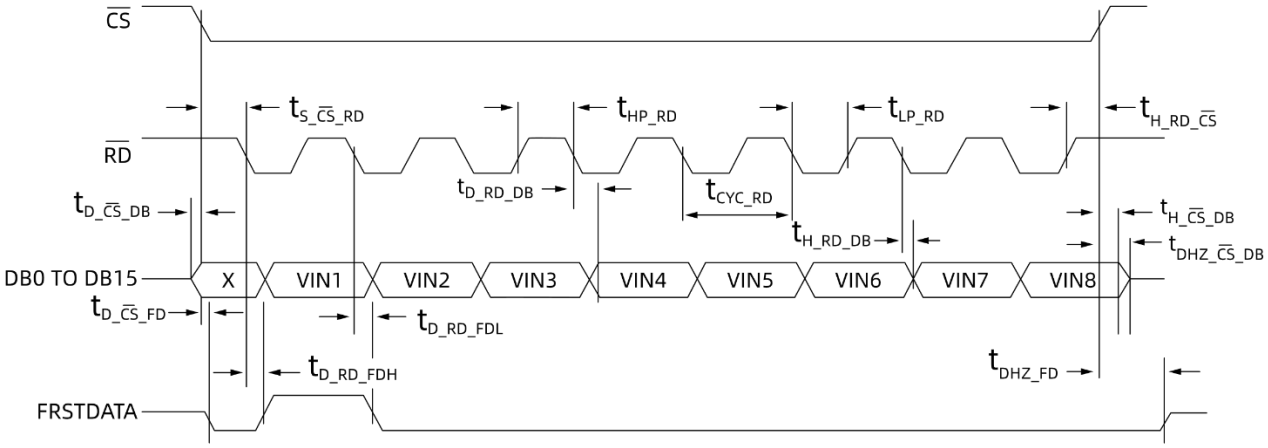


Figure 2. GD30AD3380-I10/I05 Mode Read Timing Diagram, Split $\overline{CS}$ and $\overline{RD}$ Pulse

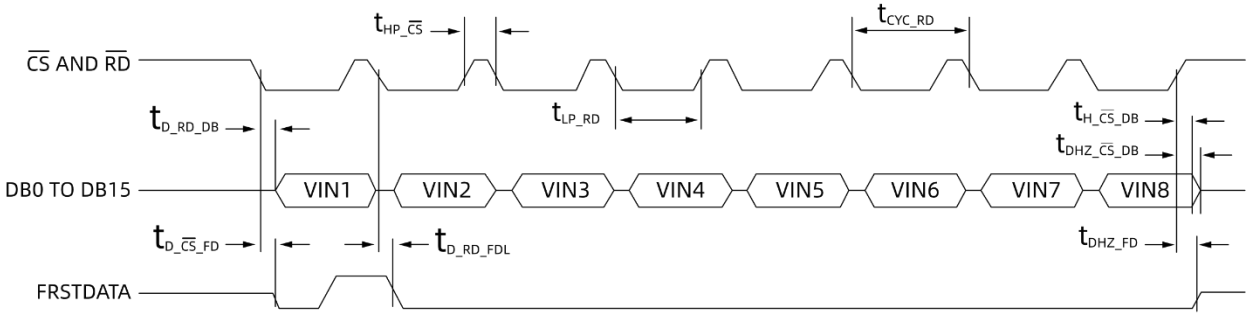


Figure 3. GD30AD3380-I10/I05 Parallel Mode Read Timing Diagram, Connected $\overline{CS}$ and $\overline{RD}$

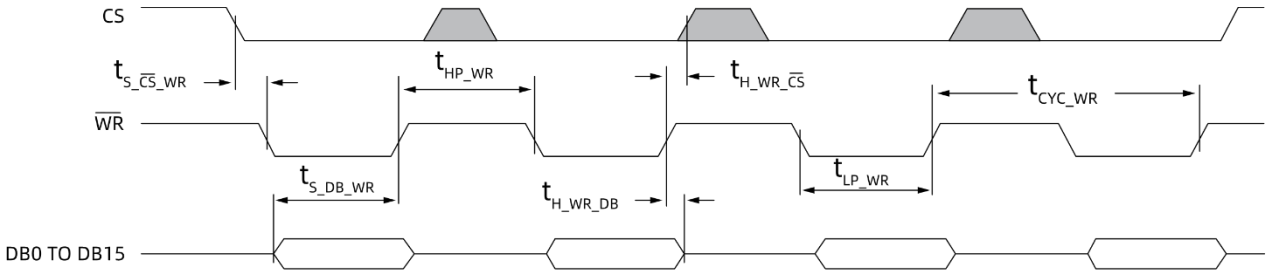


Figure 4. GD30AD3380-I10 Parallel Mode Write Operation Timing Diagram

5.5.4 Serial Mode Timing Specifications

PARAMETER	MIN	TYP	MAX	UNIT	DESCRIBE
f_{SCLK}					SCLK frequency; fSCLK = 1/t SCLK
			60	MHz	V_{DRIVE} > 2.7 V
			40	MHz	V_{DRIVE} < 2.7 V
t_{SCLK}	1/f SCLK			μs	Minimum SCLK period
$t_{S\_\overline{CS}\_SCK}$	2			ns	$\overline{CS}$ Setup time to SCLK falling edge
$t_{H\_SCK\_\overline{CS}}$	2			ns	SCLK to $\overline{CS}$ rising edge hold time
t_{LP_SCK}	0.4 x t SCLK			ns	SCLK low level pulse width
t_{HP_SCK}	0.4 x t SCLK			ns	SCLK high level pulse width
$t_{D\_\overline{CS}\_DO}$					From $\overline{CS}$ $D_{OUT}X$ to $D_{OUT}X$ tri-state disabled
			9	ns	V_{DRIVE} > 2.7 V
			18	ns	V_{DRIVE} < 2.7 V
$t_{D\_SCK\_DO}$					Data output access time after SCLK rising edge
			15	ns	V_{DRIVE} > 2.7 V
			25	ns	V_{DRIVE} < 2.7 V
$t_{H\_SCK\_DO}$	8			ns	Data output hold time after SCLK rising edge
$t_{S\_SDI\_SCK}$	8			ns	Data input setup time before SCLK falling edge
$t_{H\_SCK\_SDI}$	0			ns	Data input hold time after SCLK falling edge
$t_{DHZ\_\overline{CS}\_DO}$					$\overline{CS}$ Rising edge to $D_{OUT}X$ high impedance
			7	ns	V_{DRIVE} > 2.7 V
			twenty two	ns	V_{DRIVE} < 2.7 V
$t_{\overline{WR}}$	25			ns	Time between writing and reading the same register or between two writes; if f_{SCLK} > 50 MHz
$t_{D\_\overline{CS}\_FD}$			26	ns	From $\overline{CS}$ $D_{OUT}X$ to 3-state disabled / $\overline{CS}$ Delay time from MSB valid
$t_{D\_SCK\_FDL}$			18	ns	The 16th SCLK falls to the FRSTDATA low level
t_{DHZ_FD}			28	ns	$\overline{CS}$ Rising edge to FRSTDATA tri-state enable

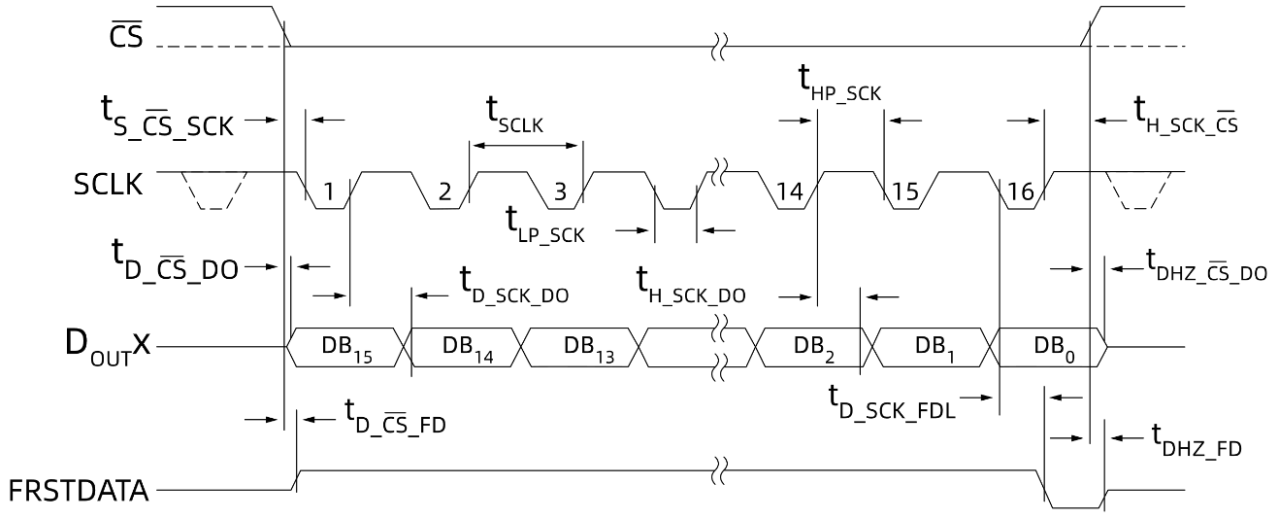


Figure 5. GD30AD3380-I10/I05 Serial Timing Diagram, ADC Read Mode (Channel 1)

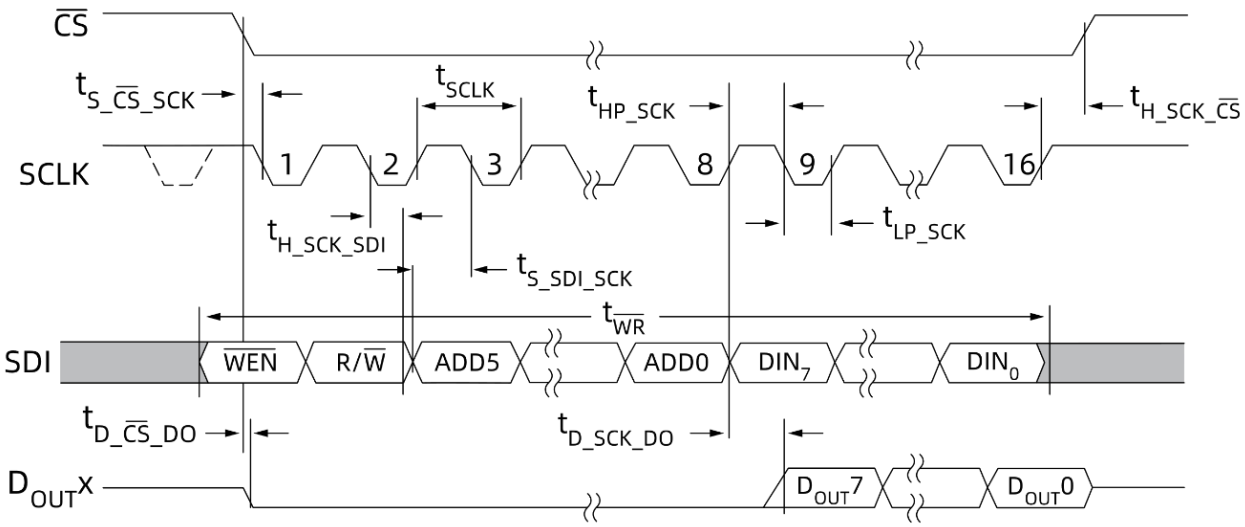


Figure 6. GD30AD3380-I10 Serial Interface Timing Diagram, Register Map Read / Write Operations

5.6 GD30AD3380-I10 Typical Characteristics

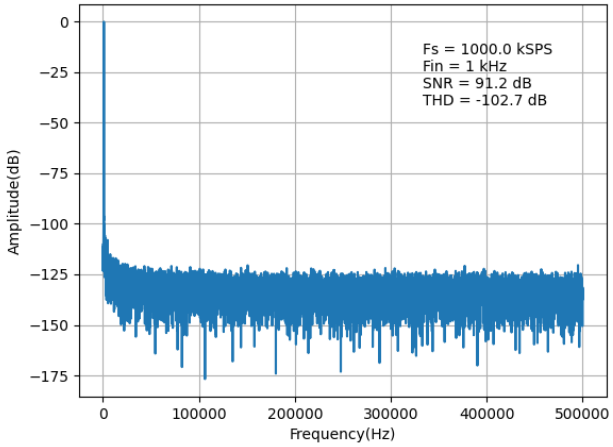


Figure 7. FFT, ±10 V Range

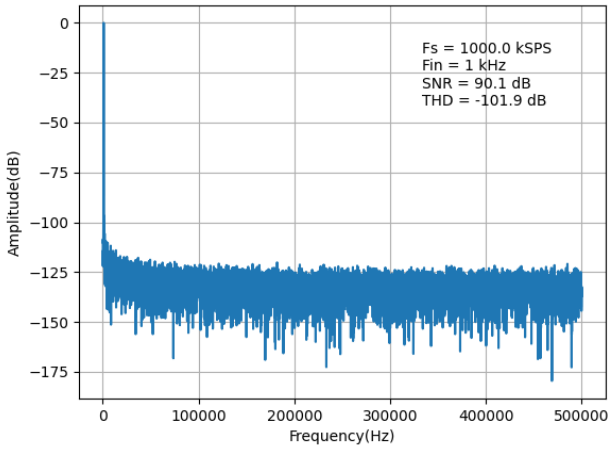


Figure 8. FFT, ±5 V Range

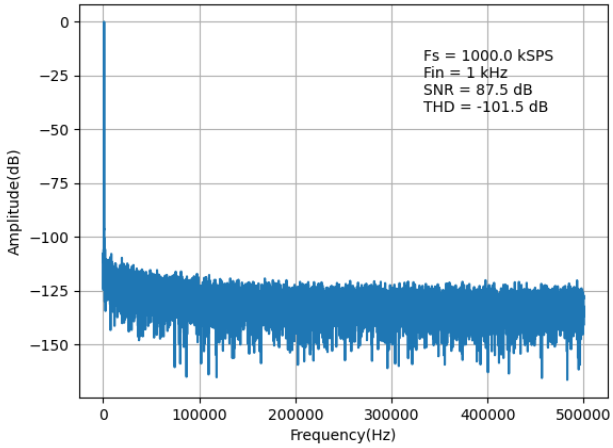


Figure 9. FFT, ±2.5 V Range

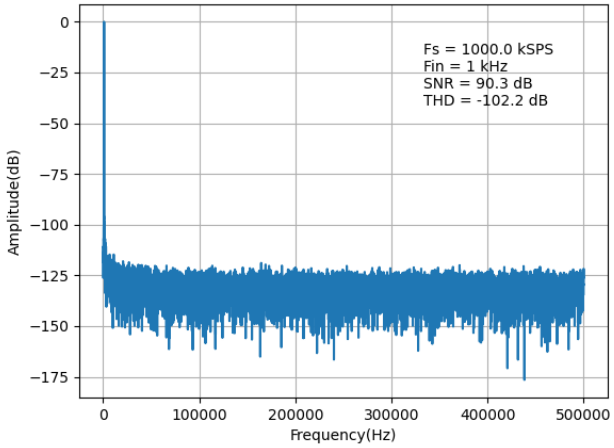


Figure 10. FFT, ±12.5 V Range

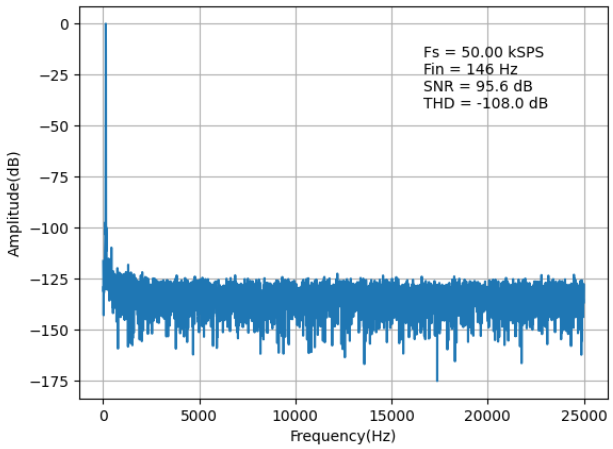


Figure 11. FFT OverSampling(16), ±10 V Range

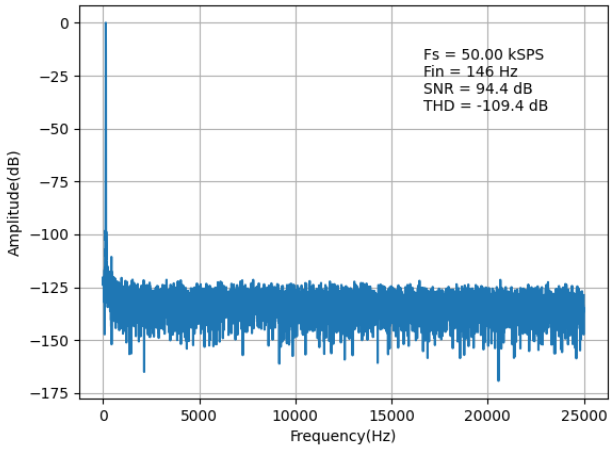


Figure 12. FFT OverSampling(16), ±5 V Range

GD30AD3380-I10 Typical Characteristic(Continued)

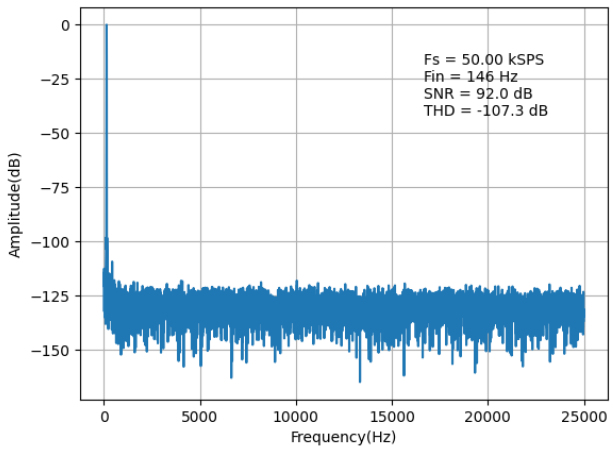


Figure 13. FFT OverSampling(16), ±2.5 V Range

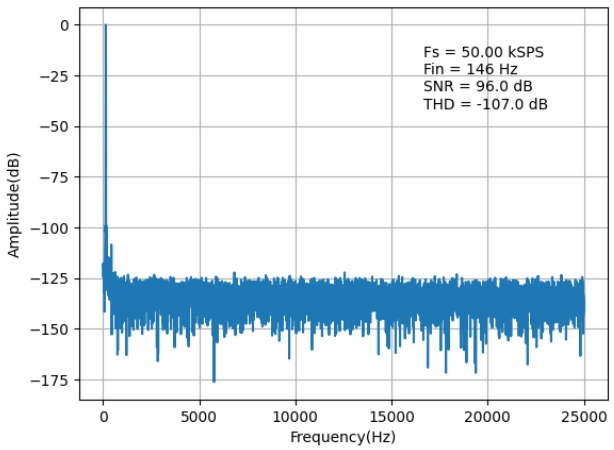


Figure 14. FFT OverSampling(16), ±12.5 V Range

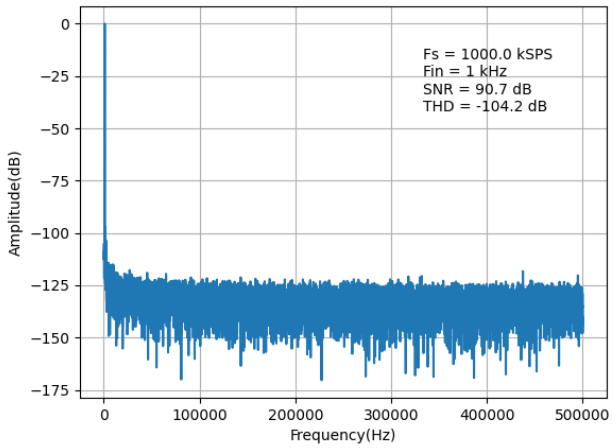


Figure 15. FFT, ±10 V Range, High Bandwidth Mode

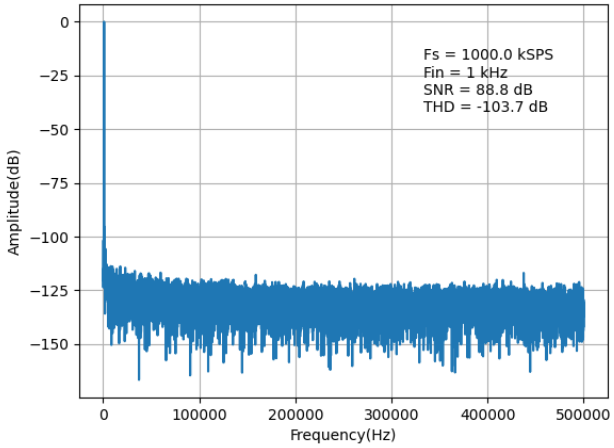


Figure 16. FFT, ±5 V Range, High Bandwidth Mode

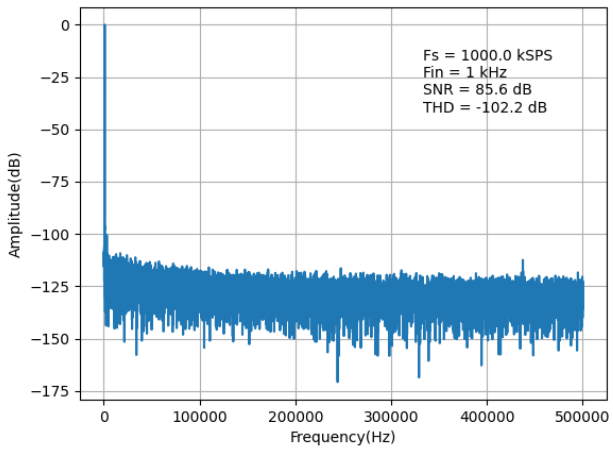


Figure 17. FFT, ±2.5 V Range, High Bandwidth Mode

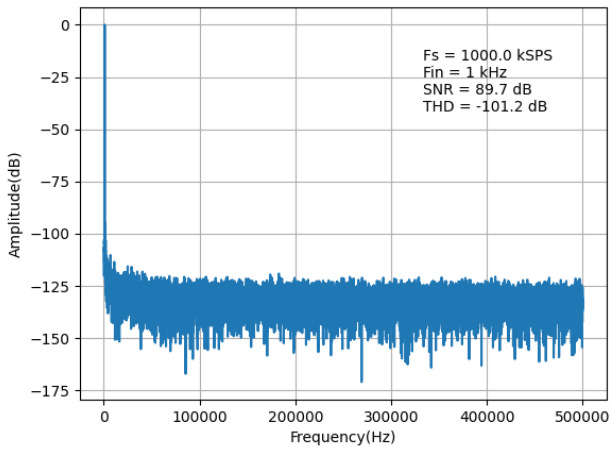


Figure 18. FFT, ±12.5 V Range, High Bandwidth Mode

GD30AD3380-I10 Typical Characteristic(Continued)

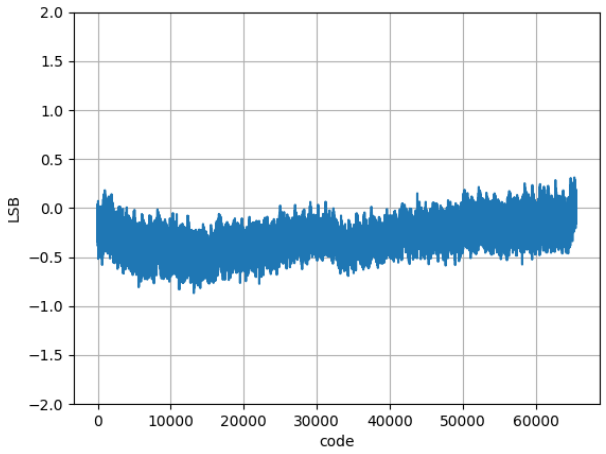


Figure 19. INL, ±10 V Range

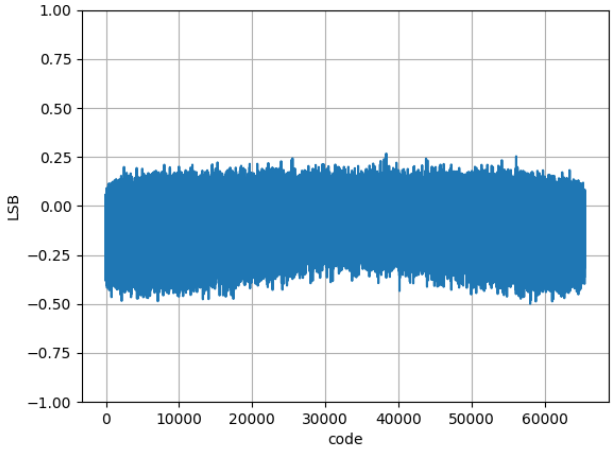


Figure 20. DNL, ±10 V Range

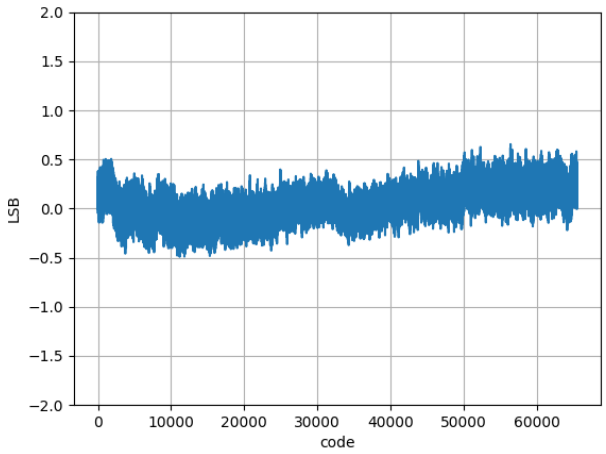


Figure 21. INL, ±5 V Range

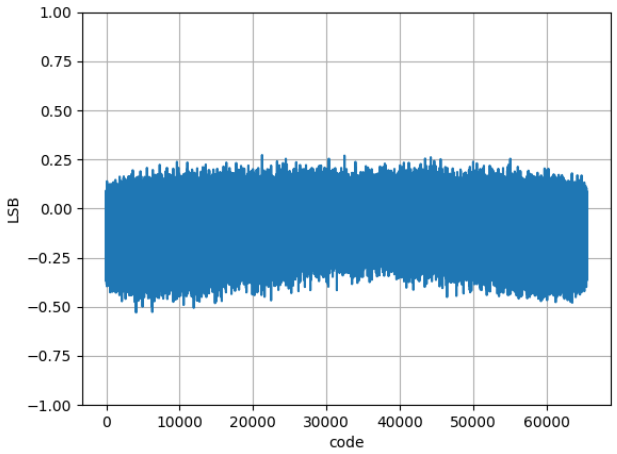


Figure 22. DNL, ±5 V Range

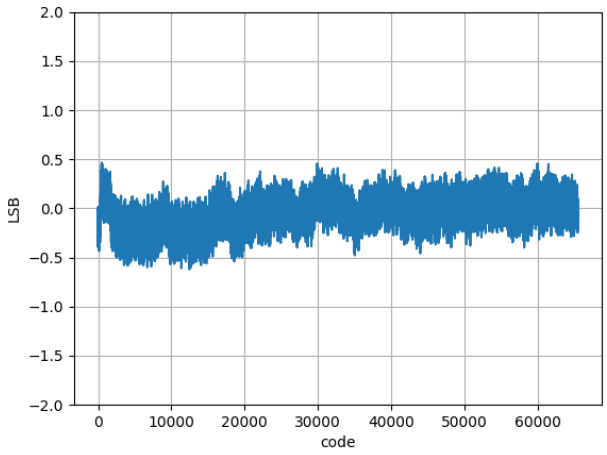


Figure 23. INL, ±2.5 V Range

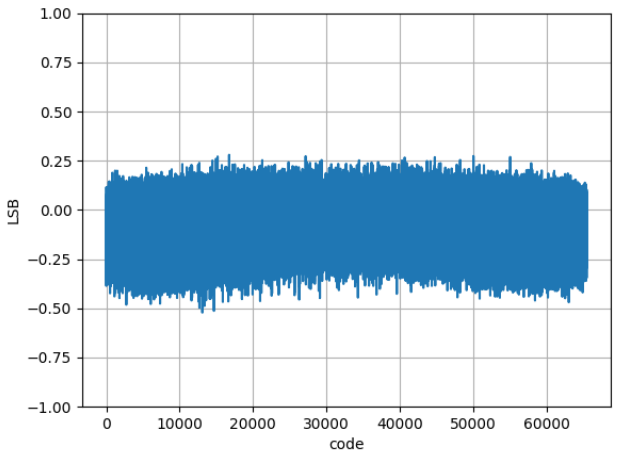


Figure 24. DNL, ±2.5 V Range

GD30AD3380-I10 Typical Characteristic(Continued)

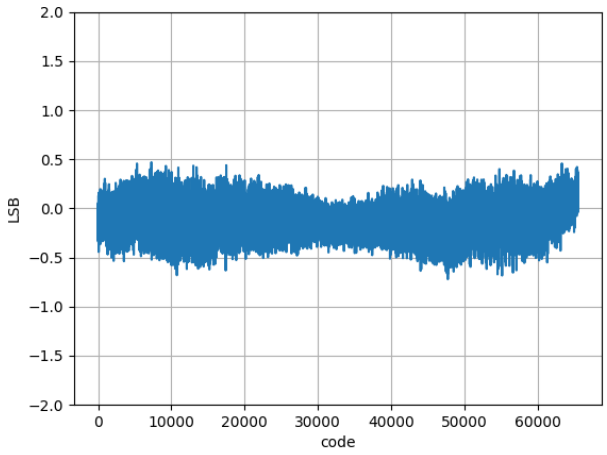


Figure 25. INL, ±12.5 V Range

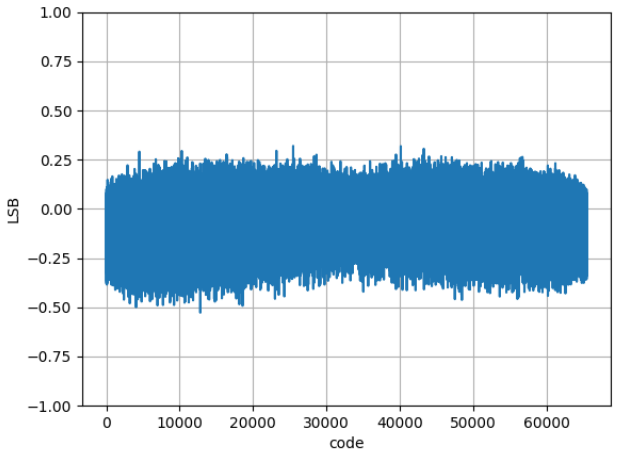


Figure 26. DNL, ±12.5 V Range

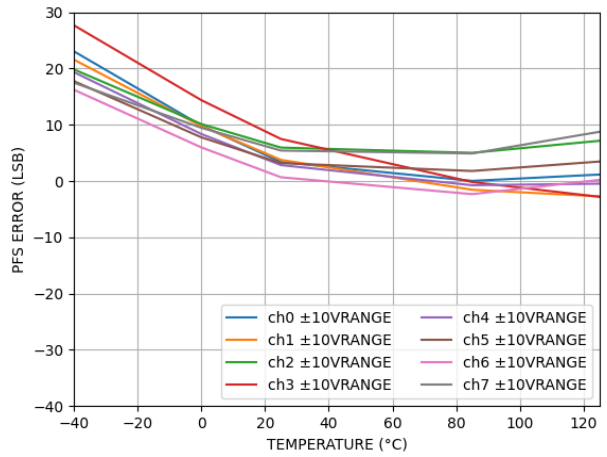


Figure 27. Full-Scale Positive Error vs. Temp, ±10 V Range

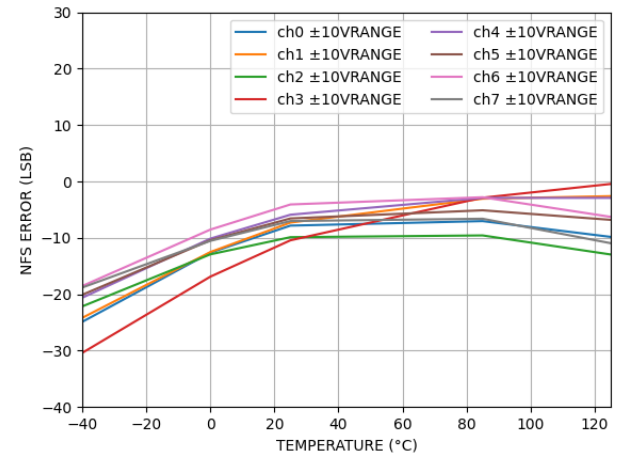


Figure 28. Full-Scale Negative Error vs. Temp, ±10 V Range

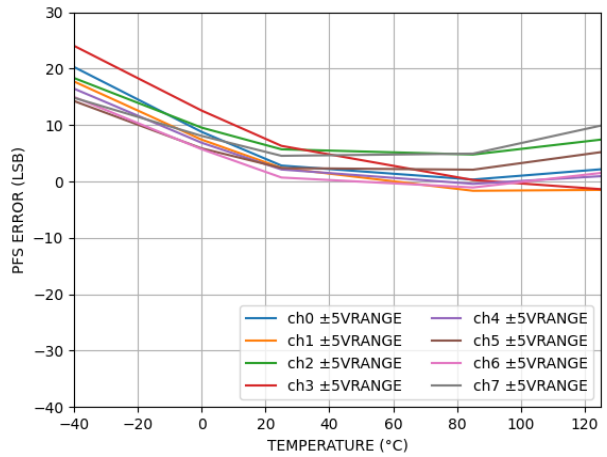


Figure 29. Full-Scale Positive Error vs. Temp, ±5 V Range

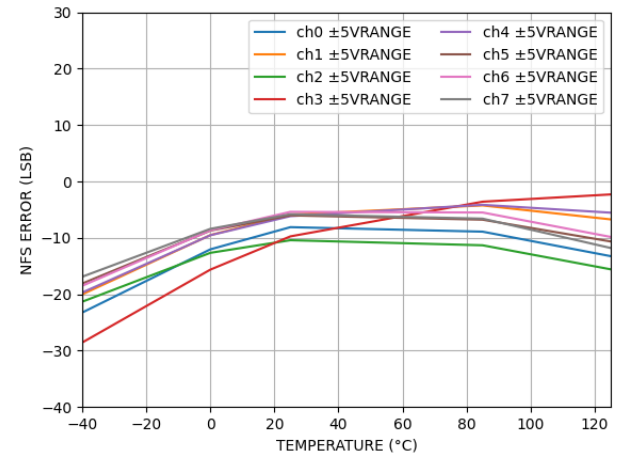


Figure 30. Full-Scale Negative Error vs. Temp, ±5 V Range

GD30AD3380-I10 Typical Characteristic(Continued)

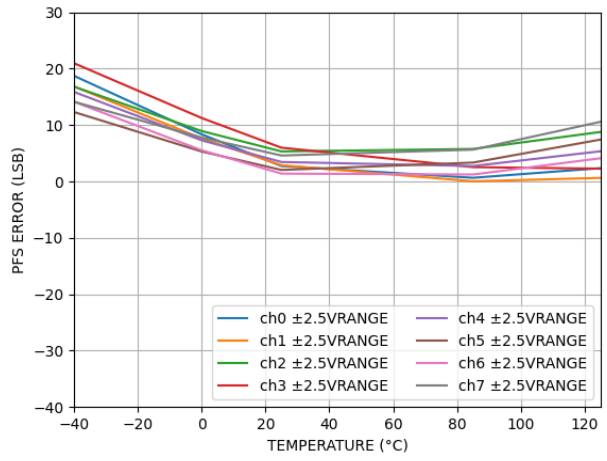


Figure 31. Full-Scale Positive Error vs. Temp, ±2.5 V Range

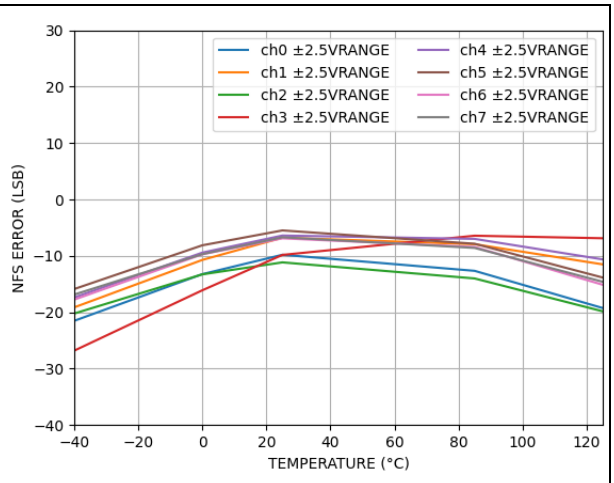


Figure 32. Full-Scale Negative Error vs. Temp, ±2.5 V Range

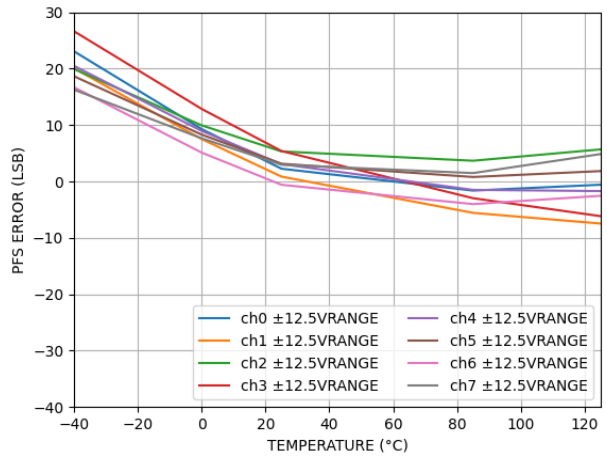


Figure 33. Full-Scale Positive Error vs. Temp, ±12.5 V Range

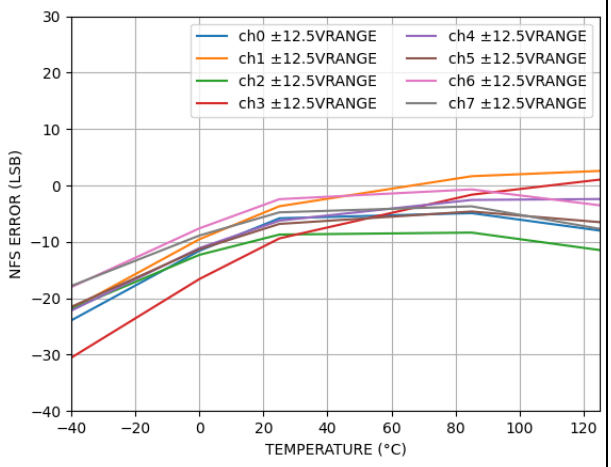


Figure 34. Full-Scale Negative Error vs. Temp, ±12.5 V Range

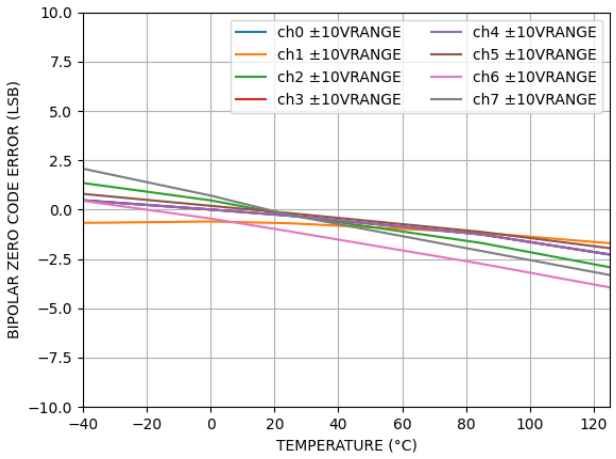


Figure 35. Bipolar Zero Code Error vs. Temp, ±10 V Range

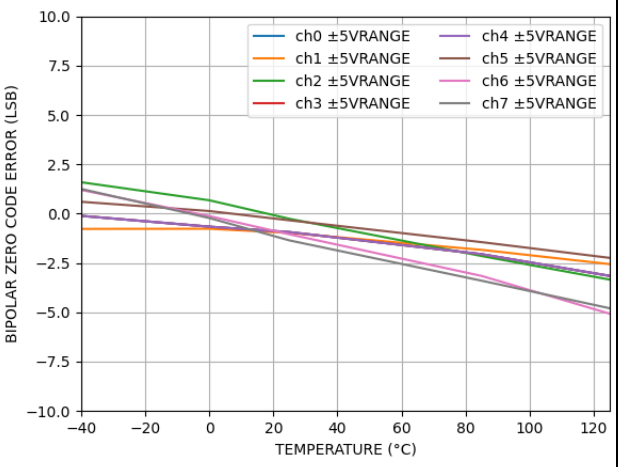


Figure 36. Bipolar Zero Code Error vs. Temp, ±5 V Range

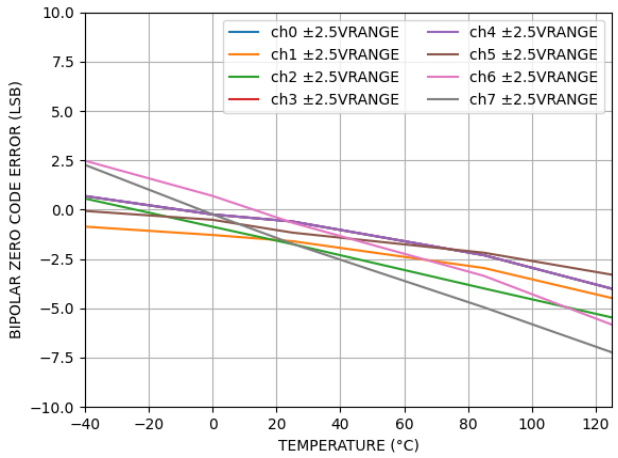


Figure 37. Bipolar Zero Code Error vs. Temp, ±2.5 V Range

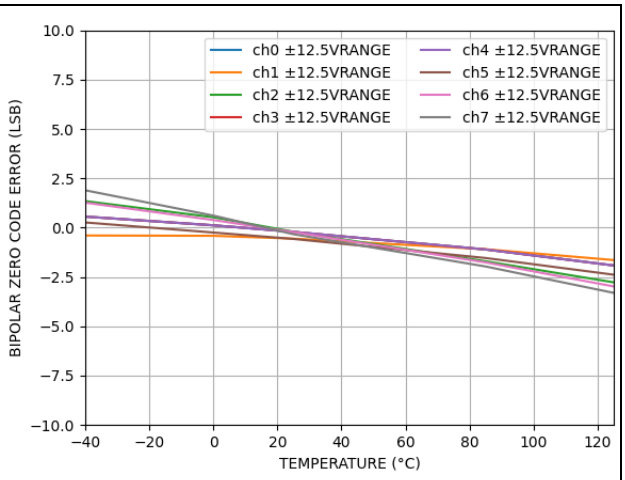


Figure 38. Bipolar Zero Code Error vs. Temp, ±12.5 V Range

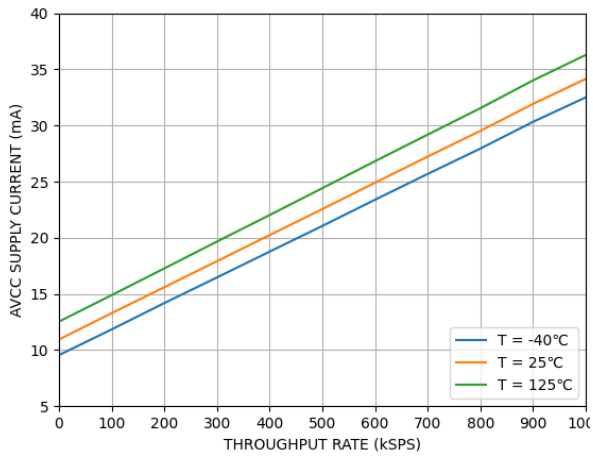


Figure 39. AVCC Supply Current vs. Sampling Rate

5.7 GD30AD3380-I05 Typical Characteristics

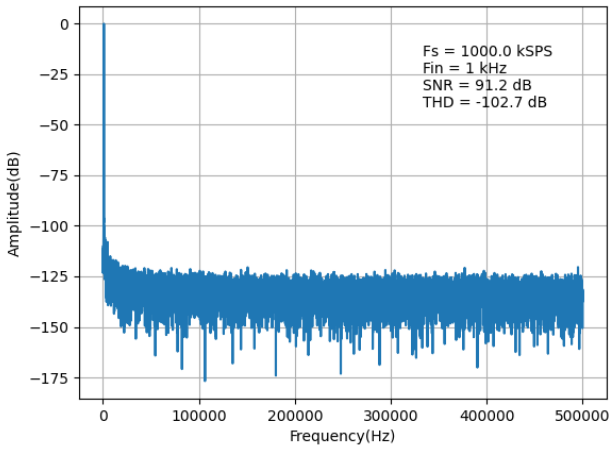


Figure 40. FFT, ±10 V Range

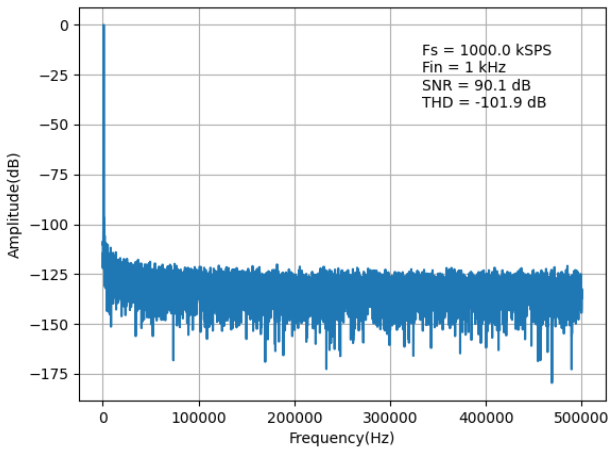


Figure 41. FFT, ±5 V Range

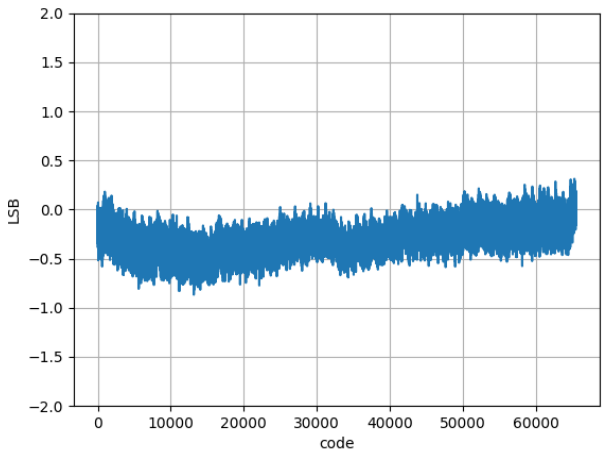


Figure 42. INL, ±10 V Range

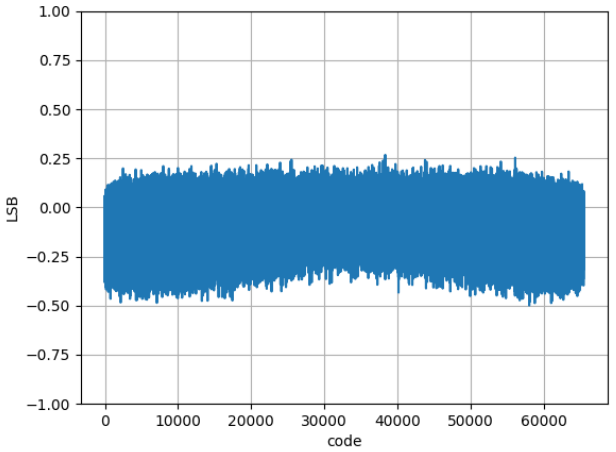


Figure 43. DNL, ±10 V Range

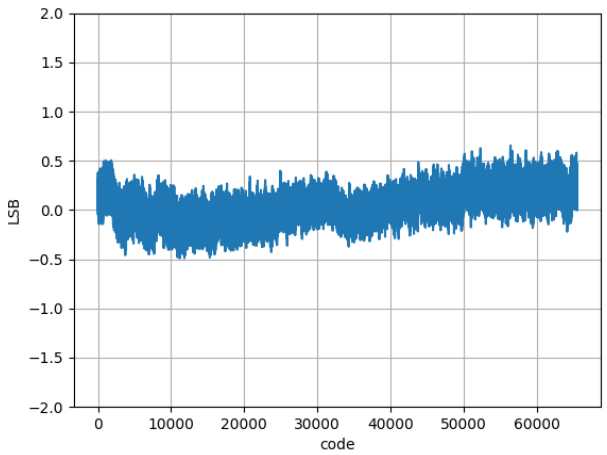


Figure 44. INL, ±5 V Range

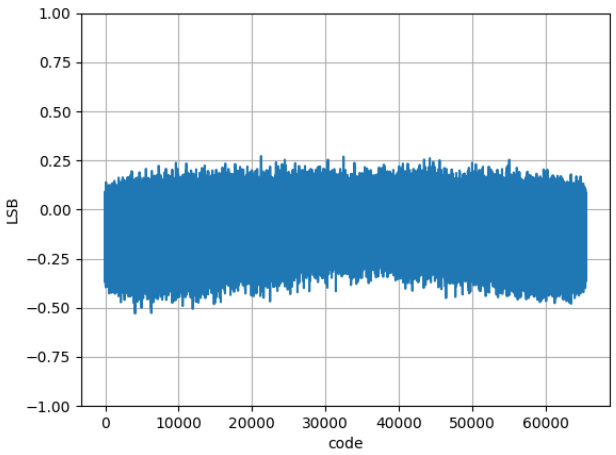


Figure 45. DNL, ±5 V Range

GD30AD3380-I05 Typical Characteristic(Continued)

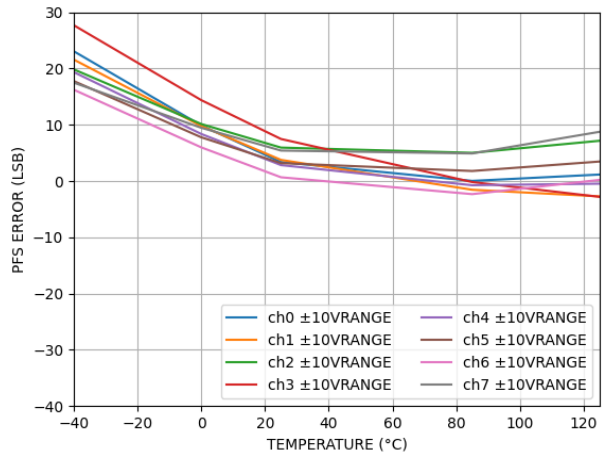


Figure 46. Full-Scale Positive Error vs. Temp, ±10 V Range

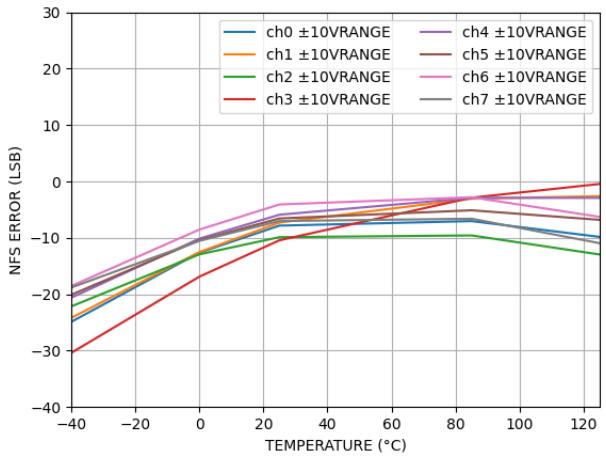


Figure 47. Full-Scale Negative Error vs. Temp, ±10 V Range

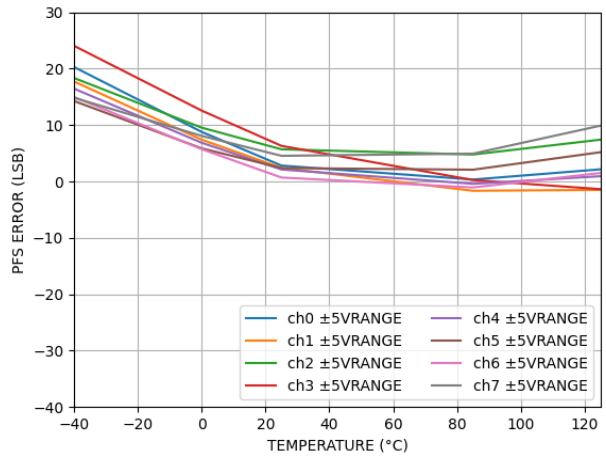


Figure 48. Full-Scale Positive Error vs. Temp, ±5 V Range

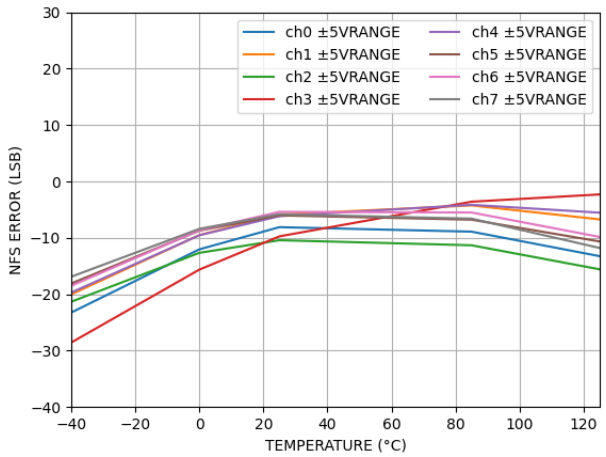


Figure 49. Full-Scale Negative Error vs. Temp, ±5 V Range

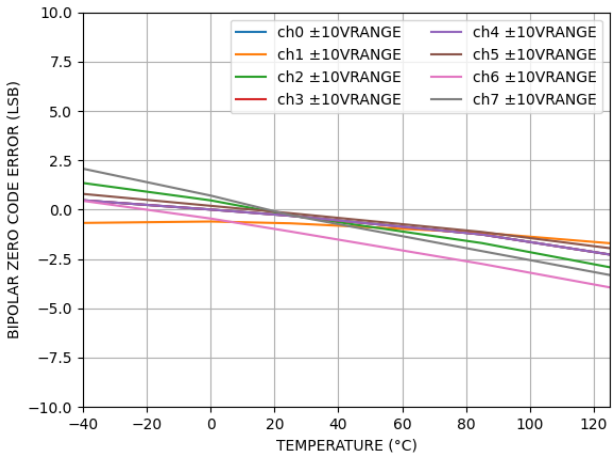


Figure 50. Bipolar Zero Code Error vs. Temp, ±10 V Range

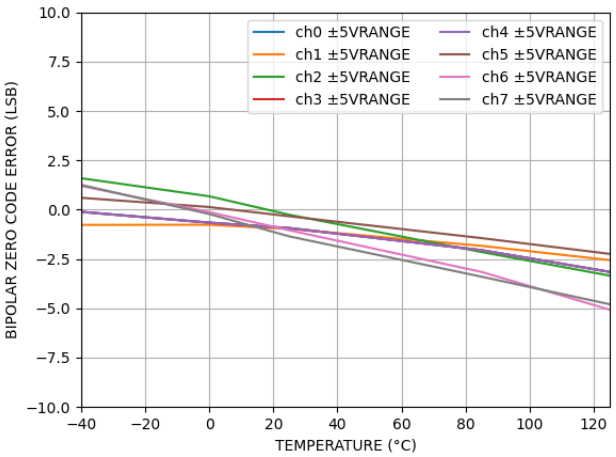


Figure 51. Bipolar Zero Code Error vs. Temp, ±5 V Range

6 Functional Description

6.1 Module Block Diagram

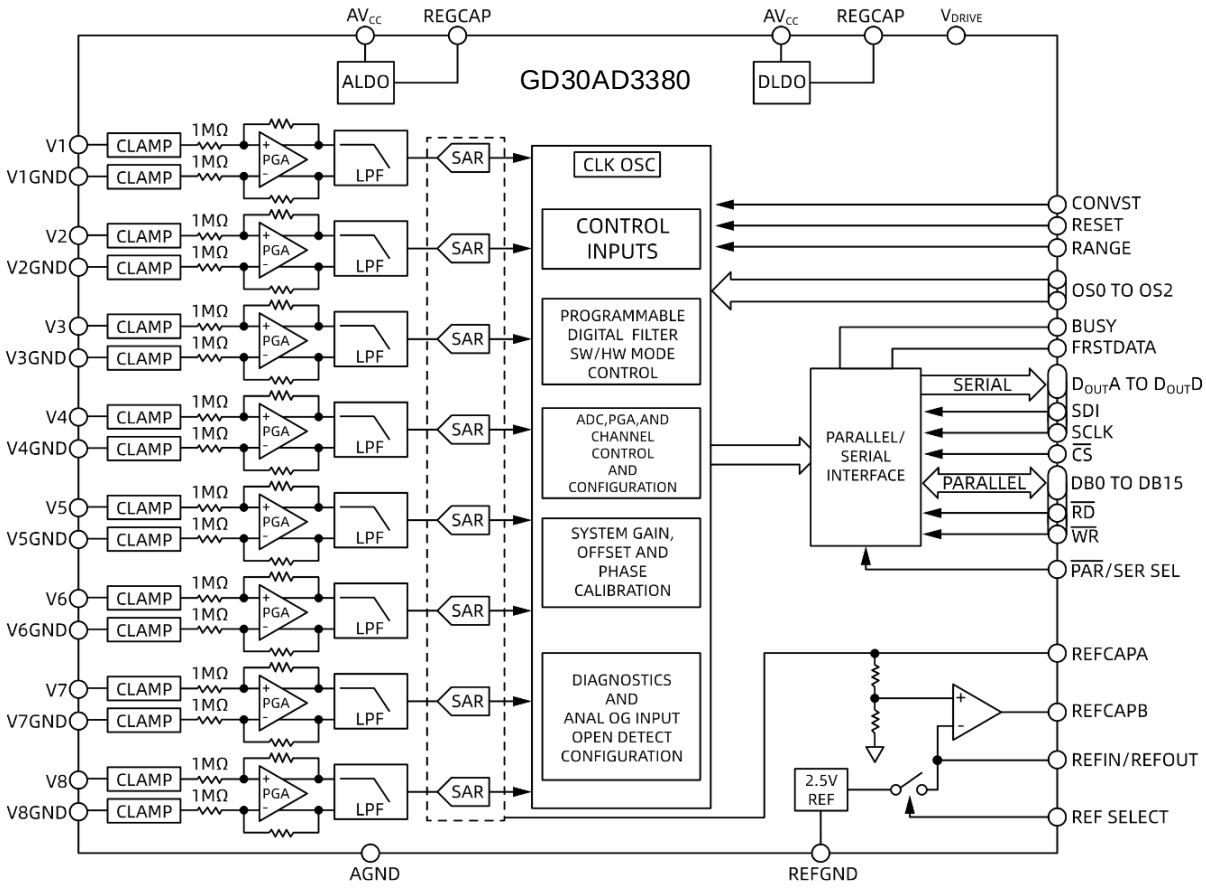


Figure 52. GD30AD3380 Block Diagram

6.2 Operation

6.2.1 Analog Front End

GD30AD3380 is a 16-bit synchronous sampling analog-to-digital converter (DAS) with 8 channels. Each channel has built-in analog input clamp protection, PGA , low-pass filter and 16-bit SAR ADC.

Analog input range

The GD30AD3380 can handle true bipolar single-ended input voltages. In hardware mode, the logic level on the RANGE pin determines whether the analog input range of all analog input channels is ±10 V or ±5 V , as shown in Table 1.

RANGE pin immediately affects the analog input range. However, a settling time of approximately 80 µs is typically required in addition to the normal acquisition time requirement . For fast throughput rate applications, it is not recommended to change the logic state of the RANGE pin during conversion .

In software mode, you can configure individual analog input ranges for each channel using Address 0x03 to Address 0x06 . The logic level on the RANGE pin is ignored in software mode.

Table 1. Analog Input Range Selection

RANGE(V)	HARDWARE MODE[1]	SOFTWARE MODE[2]
±12.5	not applicable	Address 0x03 to Address 0x06
±10	RANGE pin high level	Address 0x03 to Address 0x06
±5	RANGE pin low level	Address 0x03 to Address 0x06
±2.5	not applicable	Address 0x03 to Address 0x06

1. The same analog input range (±10 V or ±5 V) applies to all eight channels.
2. Use the memory map to select the analog input range (±10 V, ±5 V, or ±2.5 V) for each channel.

Analog input impedance

The GD30AD3380 is typically 1 MΩ . This is a fixed input impedance that does not change with the GD30AD3380 sampling frequency. The high analog input impedance eliminates the need for a driver amplifier on the front end of the GD30AD3380 , allowing it to be connected directly to a signal source or sensor. Therefore, the bipolar power supply can be removed from the signal chain.

Analog Input Clamp Protection

Figure 53 shows the analog input circuit of the GD30AD3380 . Each analog input of the GD30AD3380 contains a clamp protection circuit. This analog input clamp protection allows input overvoltages up to ±25 V despite operating from a single 5 V supply .

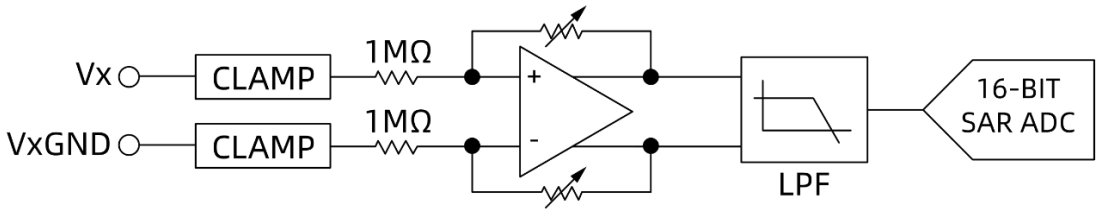


Figure 53. Analog Input Circuit for Each Channel

Figure 54 shows the input clamp current vs. source voltage characteristics of the clamp circuit. When the input voltage does not exceed ±25 V , there is no current in the clamp circuit. When the input voltage exceeds ±25 V, the GD30AD3380 clamp circuit turns on.

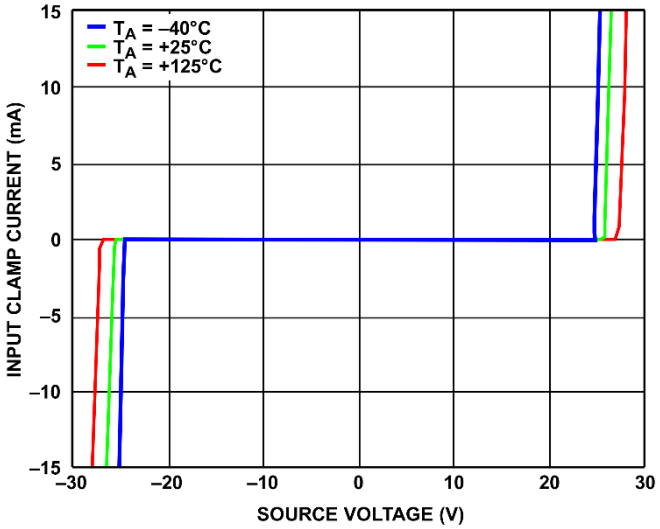


Figure 54. Input Clamp Protection Characteristics

It is recommended to place a series resistor on the analog input channel to limit the current to ±10 mA when the input voltage is greater than ±25 V. In applications where there is a series resistor (R) on the analog input channel Vx , it is recommended that the resistor (R) be matched to the resistor on VxGND to eliminate any offset introduced into the system, as shown in Figure 55. However, in software mode, a per-channel system offset calibration can eliminate the offset of the entire system (see the System Calibration *Features* section).

During normal operation, it is not recommended to subject the GD30AD3380 to conditions where the analog input is greater than the input range for extended periods of time, as this will degrade the bipolar zero code error performance. In shutdown or standby mode, there is no such concern.

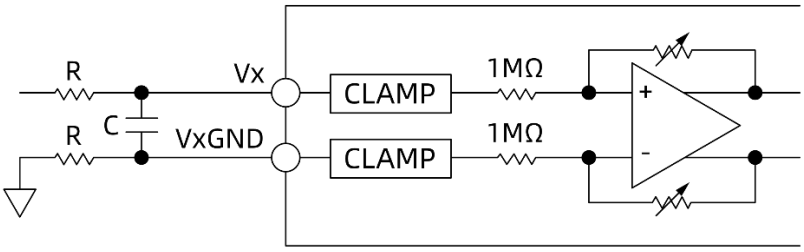


Figure 55. GD30AD3380 Analog Input

PGA

A PGA is provided for each input channel. The gain is configured based on the selected analog input range (see Table 1) to scale the single-ended analog input signal to the ADC fully differential input range.

The PGA is precisely trimmed to keep the overall gain error small. When gain calibration is enabled, this trim value is used to compensate for the gain error introduced by the external series resistors. See the *System Gain Calibration* section for more System Gain Calibrationon the PGA features .

Analog Input Anti-Aliasing Filter

GD30AD3380 provides an analog anti-aliasing filter. In the ±10 V range, the typical −3 dB bandwidth is 25 kHz . In addition, GD30AD3380 also provides a high-bandwidth mode for each channel, in which the −3dB bandwidth is increased to 200 kHz. This mode is more suitable for scenarios where fast analog input stabilization is required.

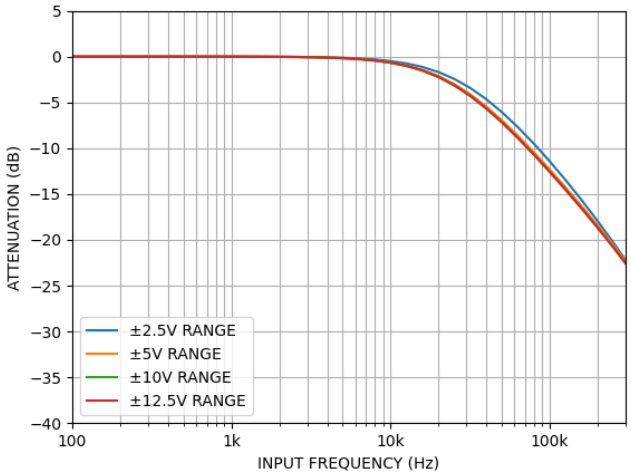


Figure 56. Analog Anti-Aliasing Filter Frequency Response, Low Bandwidth Mode

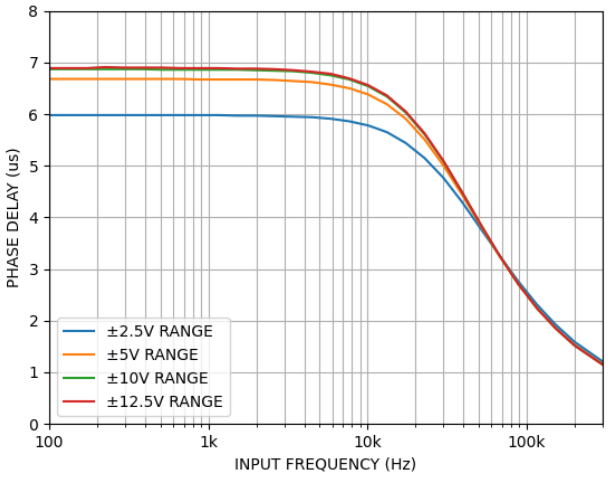


Figure 57. Analog Anti-Aliasing Filter Phase Response, Low Bandwidth Mode

Furthermore, the GD30AD3380-I10 also provides a high bandwidth mode for each channel, in which the -3dB bandwidth is increased to 200 KHz. This mode is more suitable for scenarios where fast analog input stabilization is required.

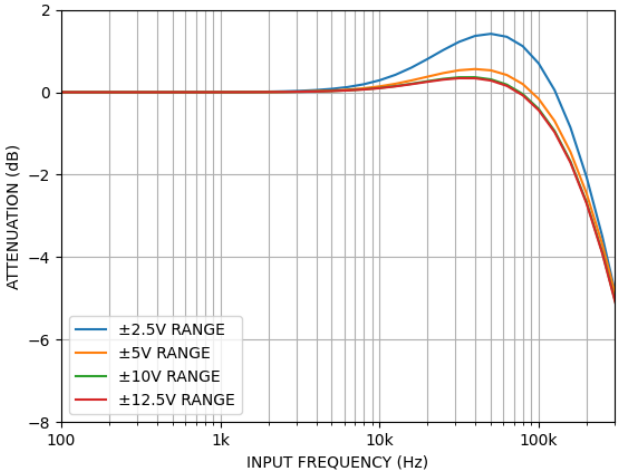


Figure 58. Analog Anti-Aliasing Filter Frequency Response, High Bandwidth Mode

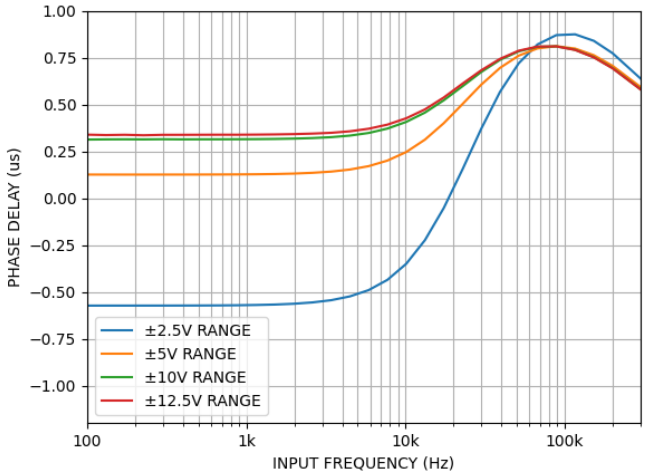


Figure 59. Analog Anti-Aliasing Filter Phase Response, High Bandwidth Mode

6.2.2 SAR ADC

The GD30AD3380 allows the ADC to accurately sample input signals with full-scale amplitude at 16-bit resolution. At the rising edge of the CONVST signal, all eight SAR ADCs sample the corresponding inputs simultaneously.

BUSY signal indicates that the conversion is in progress. Therefore, when the rising edge of the CONVST signal is applied, the BUSY pin goes to logic high and goes low at the end of the entire conversion process. The falling edge of the BUSY signal indicates the end of the conversion process for all 8 channels. When the BUSY signal falls, the acquisition time for the next set of conversions begins. When the BUSY signal is high, the rising edge of the CONVST signal has no effect.

After the BUSY output goes low, new data can be read from the output registers through the parallel or serial interface. Alternatively, previously converted data can be read while the BUSY pin is high, as described in the Reading During Conversion section .

The GD30AD3380 has an on-chip oscillator for performing conversions. The conversion time for all ADC channels is t_{CONV} (see GD30AD3380-I10 General Timing Specifications). In software mode, an external clock can be optionally applied through the CONVST pin. Providing a low-jitter external clock improves SNR performance at large oversampling rates .

Connect all unused analog input channels to AGND. The results for unused channels are still included in the data read because all channels are always converted.

ADC conversion function

The GD30AD3380 is encoded in two's complement. The designed code transitions are performed in the middle of consecutive LSB integer values (i.e., 1/2 LSB and 3/2 LSB). The LSB size of the GD30AD3380 is FSR/65,536 . The ideal transfer characteristic of the GD30AD3380 is shown in Figure 60. The LSB size depends on the selected analog input range, as shown in Table 2.

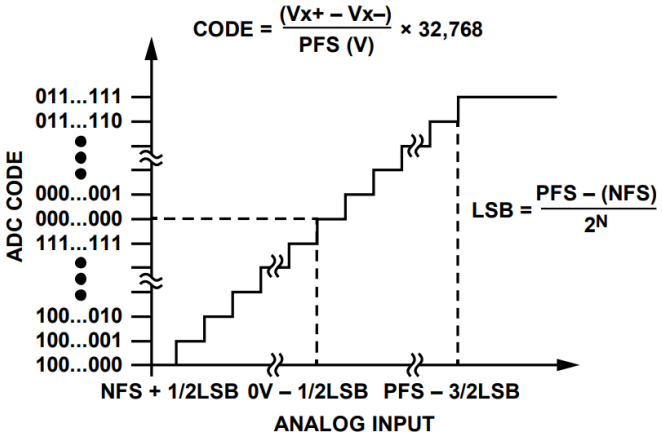


Figure 60. Ideal Transfer Characteristics

Table 2. Input Voltage Range

RANGE(V)	PFS (V)	INTERMEDIATE LEVEL(V)	NFS (V)	LSB (μV)
±12.5	+12.5	0	−12.5	381
±10	+10	0	−10	305
±5	+5	0	−5	152
±2.5	+2.5	0	−2.5	76

Voltage Reference

The GD30AD3380 has a built-in 2.5 V on-chip bandgap reference voltage source. The REFIN/REFOUT pins support the following operations:

- If the REF SELECT pin is tied to a logic high, the internal 2.5 V reference can be used.
- If the REF SELECT pin is tied to a logic low, a 2.5 V external reference voltage can be applied.

Table 3. Reference Voltage Vonfiguration

REF SELECT pin	REFERENCE SOURCE SELECTION
Logic High	Enable internal reference voltage source
Logic Low	Internal reference disabled; external 2.5 V reference must be applied to REFIN/REFOUT pins

The GD30AD3380 has a built-in reference voltage buffer configured to amplify the reference voltage to approximately 4.096 V , as shown in Figure 61. The 4.096 V buffered reference voltage is the reference voltage used by the SAR ADC , as shown in Figure 61. After reset, the GD30AD3380 operates in the reference voltage mode selected by the REF SELECT pin. The REFCAPA and REFCAPB pins must be shorted together externally and connected to the REFGND pin through a 10 μF ceramic capacitor to ensure that the reference voltage buffer operates in a closed loop. The REFIN/REFOUT pin requires a 10 μF ceramic capacitor.

When the GD30AD3380 is configured in external reference voltage mode, the REFIN/REFOUT pins are high input impedance pins.

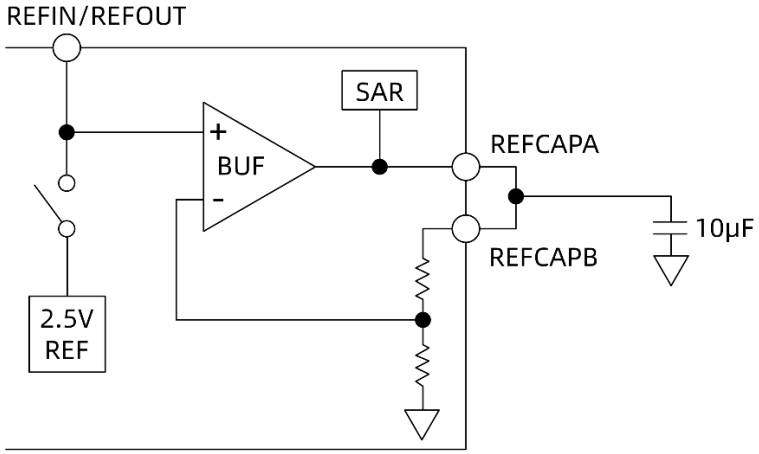


Figure 61. Reference Voltage Vircuit

Using Multiple GD30AD3380 Devices

For applications using multiple GD30AD3380 devices, the following configurations are recommended based on the application requirements.

External Reference Voltage Mode

An external reference voltage source can drive the REFIN/REFOUT pins of all GD30AD3380 devices . In this configuration, each REFIN/REFOUT pin of the GD30AD3380 should be decoupled with a decoupling capacitor of at least 100 nF .

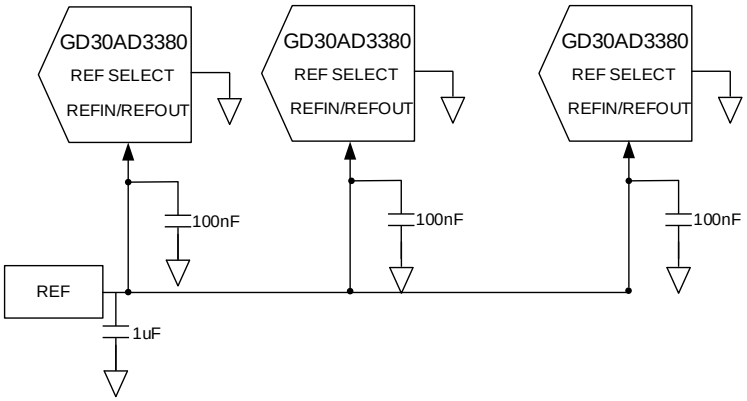


Figure 62. Single External Reference Driving Multiple GD30AD3380 REFIN/REFOUT pins

External Reference Voltage Mode

GD30AD3380 device configured in internal reference voltage operation mode can drive the remaining GD30AD3380 devices configured in external reference voltage operation mode . The GD30AD3380 configured in internal reference voltage mode should use a 10 μF ceramic decoupling capacitor to decouple its REFIN/REFOUT pins. The other GD30AD3380 devices configured in external reference voltage mode must each use a decoupling capacitor of at least 100 nF to decouple their REFIN/REFOUT pins.

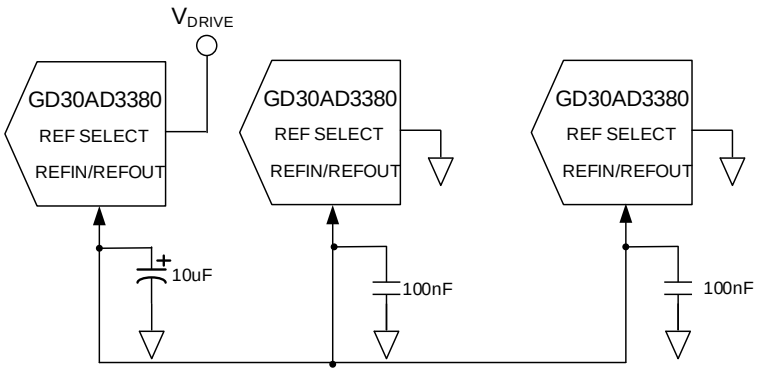


Figure 63. Internal Reference Driving Multiple GD30AD3380 REFIN/REFOUT pins

Working Mode

By controlling the OSx pins (Pin 3 , Pin 4 , and Pin 5), the GD30AD3380 can operate in hardware or software mode, as shown in Table 4In hardware mode, the configuration of the GD30AD3380 depends on the logic level of the RANGE , OSx , or $\overline{\text{STBY}}$ pins.

In software mode, that is, when all three OSx pins are connected to logic high, the GD30AD3380 is configured by the corresponding registers accessed through the serial or parallel interface. Other features are available as shown in Table 5.

In both hardware and software modes, the reference source and data interface are selected via the REF SELECT and PAR/SER SEL pins.

Table 4. Oversampling Pin Decoding

OSx PINOUT	GD30AD3380
000	No oversampling
001	2
010	4
011	8
100	16
101	32
110	64
111	Enter software mode

Table 5. Functional Matrix

PARAMETER	HARDWARE MODE	SOFTWARE MODE
Analog input range[1]	±10 V or ±5 V[2]	±12.5 V, ±10 V, ±5 V or ±2.5 V[3]
System gain, phase, and offset calibration	Unavailable	Available[3]
OSR	From no OS to OSR = 64	From No OS to OSR = 256
Analog input open circuit detection	Unavailable	Available[3]
Serial data output line	2	Available: 1, 2 or 4
diagnosis	Unavailable	supply
Power saving mode	Standby and shutdown	Standby, Off and Auto Standby

1. See Table 1 for analog input range selection.
2. All input channels are configured with the same input range.
3. On a per channel basis.

Reset function

The GD30AD3380 has two reset modes: full or partial. The reset mode selection depends on the length of the reset high pulse. Partial reset requires the RESET pin to be held high for 55 ns to 2 µs . After the RESET pin is released for 50 ns (t_{DEVICE_SETUP}, partial reset), the device is fully functional and can start conversion. Full reset requires the RESET pin to be held high for at least 3µs . After the RESET pin is released for 253 µs (t_{DEVICE_SETUP} , full reset), the device has completed reconfiguration and can start conversion.

A partial reset reinitializes the following modules:

- Digital filter.
- SPI and parallel, reset to ADC mode.
- SAR ADC .
- CRC logic.

The RESET_DETECT bit in the status register (Address 0x01 , Bit 7) is set. After the partial reset is complete, the current conversion result is discarded. A partial reset does not affect register values set in software mode or latches that store user configuration in hardware and software modes.

A full reset will restore the device to the default power-on state, the RESET_DETECT bit in the status register is set (address 0x01 bit 7), and the current conversion result is discarded. When the GD30AD3380 exits a full reset, in addition to the above, the following features are configured:

- Hardware mode or software mode.
- The interface type (serial or parallel).

Power saving mode

In hardware mode, GD30AD3380 provides two power saving modes: standby mode and shutdown mode. Table 6 $\overline{\text{STBY}}$ pin controls whether GD30AD3380 is in normal mode or one of the two power saving modes as shown below. If $\overline{\text{STBY}}$ the pin is low, the power saving mode is selected by the state of the RANGE pin.

Table 6. Power Saving Mode Selection, Hardware Mode

POWER MODE	STBY PIN	RANGE PIN
Normal Mode	1	X[1]
Standby	0	1
Shutdown	0	0

1. X = don't care.

In software mode, the power saving mode is selected by the OPERATION_MODE bits in the CONFIG register (address 0x02 bits [1:0]) in the memory map. An additional power saving mode is available in software mode, called auto-standby mode.

Table 7. Power Saving Mode Selection, Software Mode, Via CONFIG register

WORKING MODE	ADDRESS 0x02, BIT 1	ADDRESS 0x02, BIT 0
normal	0	0

WORKING MODE	ADDRESS 0x02, BIT 1	ADDRESS 0x02, BIT 0
Standby	0	1
Automatic standby	1	0
Shutdown	1	1

When the GD30AD3380 is in shutdown mode, all circuits are shut down and current consumption drops to 5 μA (max). The power-up time is approximately 10 ms . When the GD30AD3380 is powered up from shutdown mode, a full reset must be performed on the GD30AD3380 after the required power-up time .

When the GD30AD3380 enters standby mode, all PGAs and all SAR ADCs enter low power mode and the total current consumption drops to 4.5 mA (max). No reset is required after exiting standby mode.

When the GD30AD3380 is in automatic standby mode (only available in software mode), the device automatically enters standby mode at the falling edge of the BUSY signal. The GD30AD3380 automatically exits standby mode at the rising edge of the CONVST signal. Therefore, the CONVST signal low level pulse time is longer than t_{WAKE_UP} (standby mode) = 1 μs .

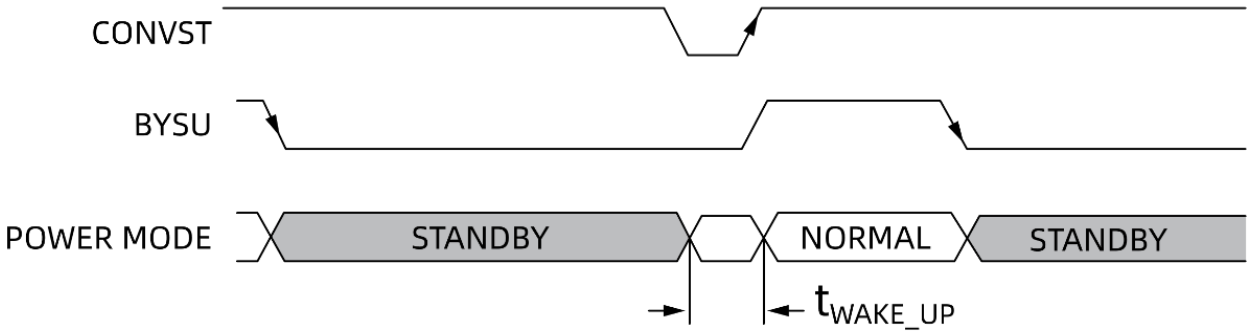


Figure 64. Automatic standby operation

7 Digital Filter

The GD30AD3380 includes an optional digital averaging filter that can be enabled in low throughput applications where higher SNR or dynamic range is required.

In hardware mode, the oversampling rate of the digital filter is controlled by the oversampling pin OSx , as Table 40The OSx pin is latched on the falling edge of the BUSY signal.

In software mode, that is, if all OSx pins are connected to logic high, the oversampling rate is selected via the oversampling register (address 0x08). Software mode provides two additional oversampling rates (OS×128 and OS×256).

In oversampling mode, the ADC acquires the first sample of each channel on the rising edge of the CONVST signal. After the first sample is converted, subsequent samples are acquired by the internally generated sampling signal, Figure 65 Alternatively , this sampling signal can be applied externally as described in the External Oversampling Clock section.

8x oversampling is configured, 8 samples are acquired, averaged, and the result is provided at the output. The rising edge of the CONVST signal triggers the first sample, and the remaining seven samples are acquired by the internally generated sampling signal. Therefore, turning on the multiple sample averaging function can improve the SNR performance at the expense of the maximum throughput rate. When the oversampling function is turned on, the high level time of the BUSY signal (t_{CONV}) is extended, as shown in GD30AD3380-I10 General Timing Specifications. Table 8 shows the relationship between SNR and bandwidth and throughput rate for the ±10 V , ±5 V , and ±2.5 V ranges .

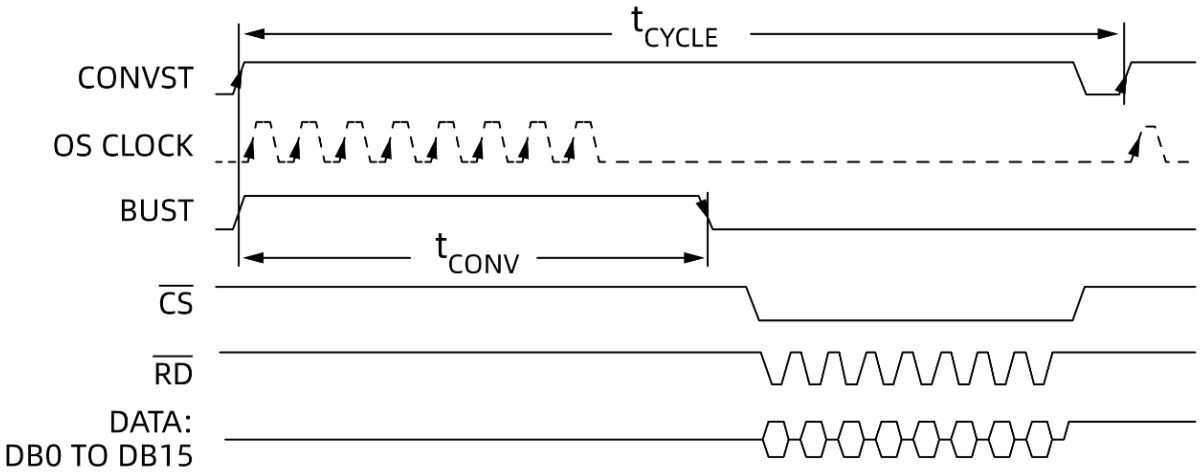


Figure 65of 8x oversampling, read after conversion, parallel interface, sampling signal generated internally by OS clock

Figure 65 (t_{CONV}) increases when oversampling is turned on . The throughput rate ($1/t_{CYCLE}$) must be reduced to accommodate the longer conversion time and allow read operations to be performed. When oversampling is turned on, to achieve the fastest throughput rate, read operations can be performed during the high period of the BUSY signal, as described in the Reading During Conversion section .

Table 8. Oversampling Performance

Oversampling rate	Input frequency (Hz)	±12.5V range		±10 V range		±5 V range		±2.5 V range		Throughput rate (kSPS)
		SNR (dB)	3 dB Bandwidth (kHz)	SNR (dB)	3 dB Bandwidth (kHz)	SNR (dB)	3 dB Bandwidth (kHz)	SNR (dB)	3 dB Bandwidth (kHz)	
No oversampling	1000	91.5	23.0	91.5	23.0	90	13.9	87	11.6	800
2	1000	93.5	22.7	93	22.7	91.5	13.8	88	11.5	400
4	1000	94.5	22.0	94	22.0	92.5	13.6	89	11.4	200
8	1000	95	20.0	94.5	20.0	93	13.0	90	11.1	100
16	146	96	15.4	95.5	15.4	94	11.4	92	10.0	50
32	146	96	9.7	95.5	9.7	95	8.4	93	7.7	25
64	146	96	5.3	96	5.3	95.5	5.0	94	4.9	12.5

Oversampling rate	Input frequency (Hz)	±12.5V range		±10 V range		±5 V range		±2.5 V range		Throughput rate (kSPS)
		SNR (dB)	3 dB Bandwidth (kHz)	SNR (dB)	3 dB Bandwidth (kHz)	SNR (dB)	3 dB Bandwidth (kHz)	SNR (dB)	3 dB Bandwidth (kHz)	
128 [1]	146	96	2.7	96	2.7	95.5	2.7	95	2.7	6.25
256 [1]	146	96	1.4	96	1.4	95.5	1.4	95.5	1.4	3.125

1. Available only in software mode.

7.1 Fill Oversampling

Figure 66, the internally generated clock triggers the samples to be averaged, and then the ADC remains idle until the next rising edge of the CONVST signal. In software mode, the internal clock (OS clock) frequency can be changed through the oversampling register (address 0x08 to minimize the idle time, that is, to make the sampling moments evenly distributed, as shown in Figure 66.

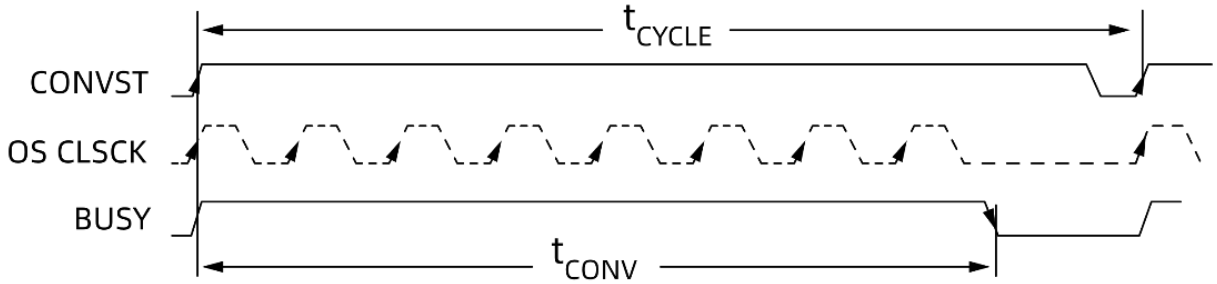


Figure 66. 8x Oversampling Example, Oversampling Padding Enabled

Table 9. OS_PAD Bit Decoding

OS_PAD (ADDRESS 0x08, BITS [7:5])	OS CLOCK FREQUENCY (kHz)
0000	800
0001	753
0010	711
0011	673.5
0100	640
0101	609.5
0110	582
0111	556.5
1000	533
1001	512
1010	492.5
1011	474
1100	457
1101	441.5
1110	426.5
1111	413

7.2 External Oversampling Clock

In software mode, when oversampling mode is enabled, an external clock can be optionally applied through the CONVST pin. Providing a low jitter external clock improves SNR performance at large oversampling ratios . By applying an external clock, the input is sampled at regular time intervals, which is optimal for anti-aliasing performance.

To enable the external oversampling clock, Bit 5 of the CONFIG register must be set (Address 0x02 Bit 5).

This gives a throughput rate of

$$\text{Throughout} = \frac{1}{t_{CNVST} \times OSR} \quad (1)$$

That is, the sampling signal is provided externally through the CONVST pin, and the output is averaged and provided every Figure 67 OSR clocks, as shown in Figure 67. This feature can be used through either the parallel interface or the serial interface.

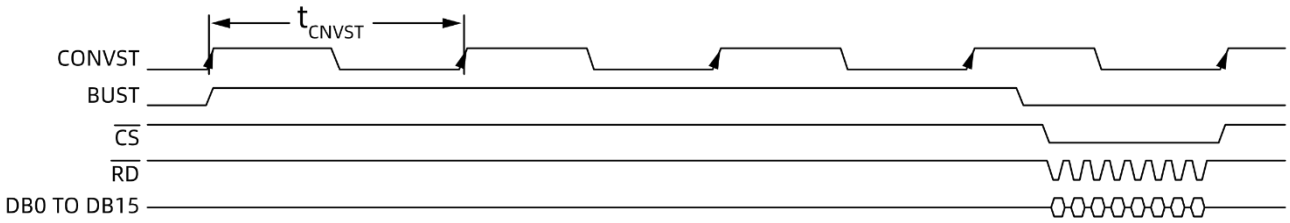


Figure 67. External Oversampling Clock Applied to CONVST Pin (OSR = 4); Parallel Interface

8 System Calibration Features

In software mode, the following system calibration features are available by writing to the appropriate registers in the memory map:

- Phase calibration.
- Gain calibration.
- Offset calibration.
- Analog input open circuit detection.

8.1 System Phase Calibration

When using external filters, any mismatch in the discrete components or the sensors used can result in a phase mismatch between the channels, as shown in Figure 69. In software mode, this phase mismatch can be compensated on a per-channel basis by delaying the sampling instant of the individual channels.

The sampling instant for any particular channel can be delayed relative to the rising edge of the CONVST signal with a resolution of 1.25 µs up to a maximum of 318.75 µs by writing to the corresponding CHx_PHASE register (Address 0x19 to Address 0x20).

For example, if 10d is written to the CH4_PHASE register (address 0x1C) , channel 4 is sampled 12.5µs (t_{PHASE_REG}) after the rising edge of the CONVST signal , as shown in Figure 68.

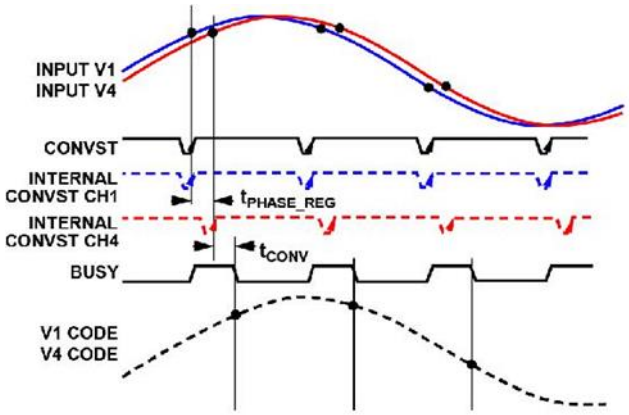


Figure 68System phase calibration function

BUSY signal high time is equal to t_{CONV} + t_{PHASE_REG} , as shown in Figure 68. In the example described previously and in Figure 68, if only CH4_PHASE_REGISTER is written , t_{CONV} increases by 12.5 µs . Therefore, this situation must be taken into account when running at higher throughput rates.

8.2 System Gain Calibration

Using an external RFILTER will result in a system gain error, as shown in Figure 69. In software mode, the gain error can be compensated on a per-channel basis by writing the series resistor value used into the appropriate registers (Address 0x09 to Address 0x10). These registers can compensate for series resistances up to 65 kΩ with a resolution of 1024 Ω .

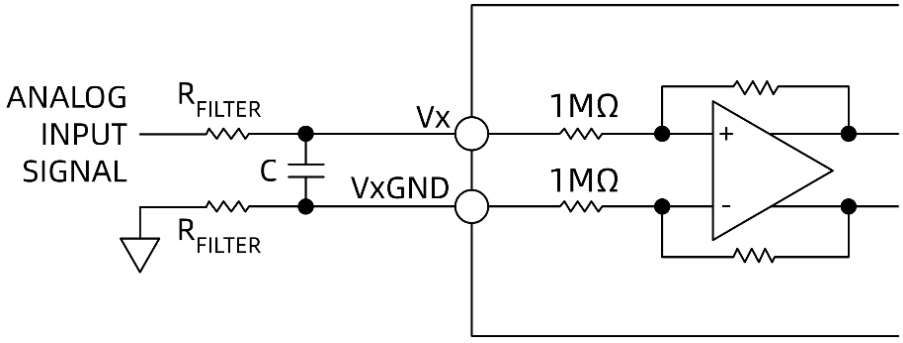


Figure 69. System Gain Error

For example, if a 27 kΩ resistor is placed in series with the analog input of Channel 5 , the resistor will create a -170 LSB positive full-scale error (±10 V range) in the system, as shown in Figure 70. In software mode, writing 27d to the CH5_GAIN register (Address 0x0D) eliminates this error.

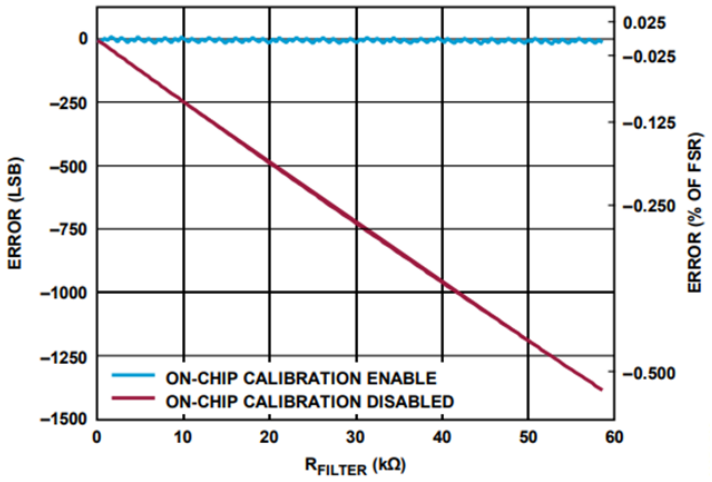


Figure 70. System Gain Calibration with and without Calibration

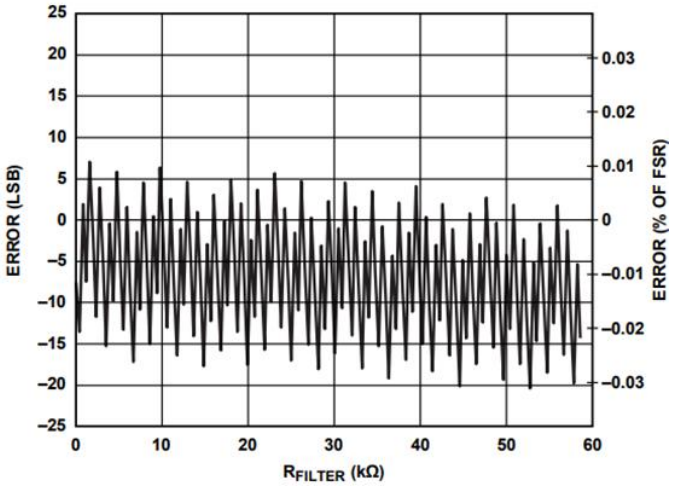


Figure 71. Systematic Error in Gain Calibration

8.3 System Offset Calibration

Any offset caused by a mismatch between the RFILTER pairs placed on a particular channel (as described in the *Analog Front End* section), can be compensated on a per-channel basis in software mode. The CHx_OFFSET registers (Address 0x11 to Address 0x18) support automatic addition or subtraction of up to 128 LSBs from the ADC code with a resolution of 1 LSB , as shown in Table 10.

For example, if the signal connected to Channel 3 has a 9 mV offset and the analog input range is set to the ±10 V range (where LSB size = 305 µV), to compensate for this offset, −30 LSB should be written to the appropriate register. This offset can be removed by writing 128d − 30d = 0x80 − 0x1E = 0x62 to the CH3_OFFSET register (Address 0x13).

Table 10. CHx_OFFSET Register Bit Decoding

CHx_OFFSET Register	Offset Calibration (LSB)
0x00	−128
0x45	−59
0x80 (default)	0
0x83	+3
0xFF	+127

8.4 Analog Input Open Circuit Detection

The GD30AD3380 has an analog input open circuit detection feature that can be used in software mode. To use this feature, $R_{PD\ must}$ be placed as shown in Figure 72. If the analog input is disconnected, such as Figure 72 changes from R_S to R_{PD} as long as $R_S < R_{PD}$. It is recommended to use R_{PD} = 50 kΩ so that the GD30AD3380 can detect the change in source impedance by internally switching the PGA common-mode voltage. Analog input open circuit detection works in manual mode or automatic mode in software mode.

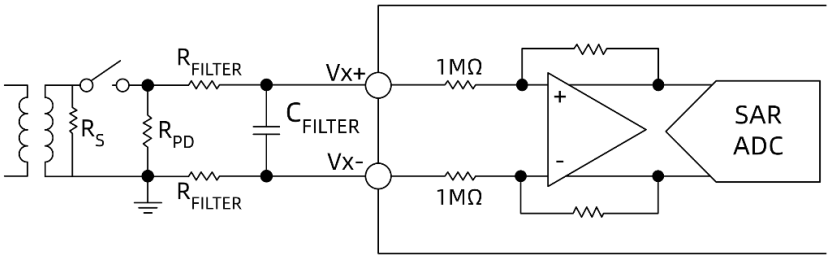


Figure 72. Analog Front End with R_{PD}

Manual Mode

In manual mode (enabled by writing 0x01 to OPEN_DETECT_QUEUE (Address 0x2C), each PGA common-mode voltage is set by the OPEN_DETECT_ENABLE register. live Device (ground The ADC common-mode voltage is controlled by the corresponding CHx_OPEN_DETECT_EN bit in the analog input (address 0x23) . Setting this bit high will shift the PGA common-mode voltage up. If there is an open circuit on the analog input, the ADC output will change proportionally to the R_{PD} resistance. If there is no open circuit, any change in the PGA common-mode voltage will not affect the ADC output.

Automatic mode

QUEUE (specified in the register) for consecutive unchanged conversion results, the analog input open-circuit detection algorithm is automatically executed internally. The analog input open-circuit detection algorithm automatically changes the PGA common-mode voltage, checks the ADC output, and returns to the initial common-mode voltage, as shown in Figure 73. If the ADC code in any channel changes with the PGA common-mode voltage change, it means that there is no input signal connected to that analog input, and the corresponding flag in the OPEN_DETECTED register (Address 0x24) is set. Each channel can be enabled or disabled individually through the OPEN_DETECT_ENABLE register (Address 0x23).

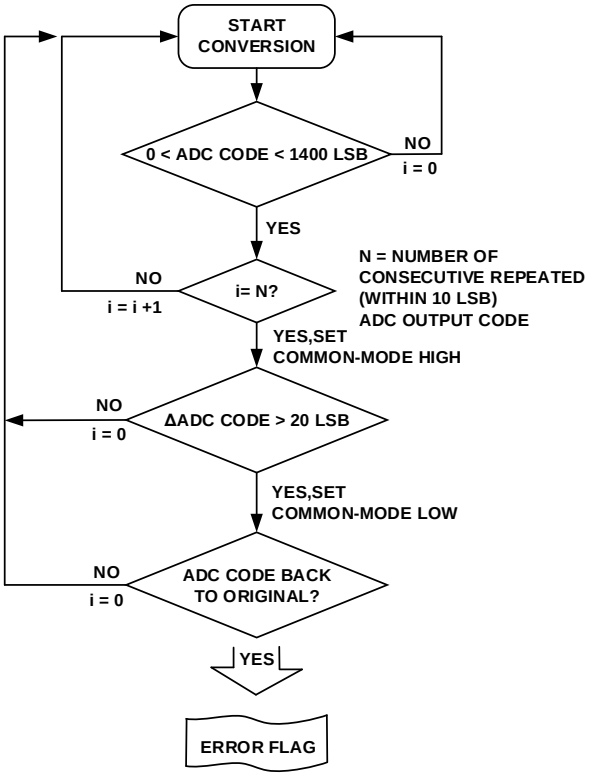


Figure 73. Automatic Analog Input Open Circuit Detection Flow Chart

If oversampling is not used, the recommended minimum number of conversions to be written to the GD30AD3380 for automatic detection of an analog input open circuit is:

$$OPEN\_DETECT\_QUEUE = 10 \times f_{sample} \left(R_{PD} + 2 \times R_{FILTER}\right) \times \left(C_{FILTER} + 10pF\right) \quad (2)$$

However, if oversampling mode is enabled, the minimum recommended number of conversions is:

$$OPEN\_DETECT\_QUEUE = 1 + \left(f_{sample} \times 2 \times \left(R_{PD} + 2 \times R_{FILTER}\right) \times \left(C_{FILTER} + 10pF\right) \times OSR\right) \quad (3)$$

Table 11. OS_PAD bit decoding

OPEN_DETECT_QUEUE (Address 0x2C)	Open circuit detection mode	OPEN_DETECT_ENABLE (Address 0x23)
0x00 (default)	Disable	not applicable
0x01	Manual Mode	Set the common mode voltage to high or low on a per channel basis
0x02 to 0xFF	Automatic; OPEN_DETECT_QUEUE is the number of consecutive conversions. When this number is reached, the CHx_OPENED flag will be set.	Enable or disable automatic analog input open wire detection on a per channel basis

9 Digital Interface

GD30AD3380 provides two interface options: parallel interface and high-speed serial interface. The required interface mode can be selected through the PAR/SER SEL pin.

Table 12. Interface Mode Selection

PAR/SER SEL	Interface Mode
0	Parallel interface mode
1	Serial interface mode

The following sections discuss how these interface modes work.

9.1 Hardware Mode

In hardware mode, only ADC read mode is available. To read ADC data from the GD30AD3380 , you can do so through the parallel data bus and use the standard $\overline{CS}$ and $\overline{RD}$ signals, or through the serial interface and use the standard $\overline{CS}$, SCLK , and two D_{OUT}X signals.

For more information on how the ADC read mode works, refer to the Reading Conversion Results (Parallel ADC Mode) section and the Reading Conversion Results (Serial ADC Mode) section .

9.2 Software Mode

In software mode (valid only when all three oversampling pins are tied high), both ADC read mode and register mode are available. ADC data can be read from the GD30AD3380 , and registers can also be read and written to the GD30AD3380 , through the parallel data bus and using standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ signals, or through the serial interface and using standard $\overline{CS}$, SCLK , SDI , and D_{OUT} lines .

For more information about how register mode works, see the Parallel Register Mode (Writing Register Data) section and the Parallel Register Mode (Reading Register Data) section .

The pin functions vary depending on the selected interface (parallel or serial) and operating mode (hardware or software), as shown in Table 13 and Table 14.

Table 13. Data Interface Pin Functions for Each Operating Mode (Parallel Interface)

Pin Name	Pin Number	Hardware Mode	Software Mode	
			ADC Mode	Register Mode
DB0 to DB6	16 to 22	DB0 to DB6		Register data
DB7/D_{OUT}A	24	DB7		Register data (MSB)
DB8/D_{OUT}B	25	DB8		ADD0
DB9/D_{OUT}C	27	DB9		ADD1
DB10/D_{OUT}D	28	DB10		ADD2
DB11/SDI	29	DB11		ADD3
DB12 to DB14	30 to 32	DB12 to DB14		ADD4 to ADD6
DB15	33	DB15		R/W

Table 14. Data Interface Pin Functions for Each Operating Mode (Serial Interface)

Pin Name	Pin Number	Hardware Mode	Software Mode	
			ADC Mode	Register Mode
DB0 to DB6	16 to 22	N/A[1]	N/A	
DB7/DOUTA	24	DOUTA	DOUTA	DOUTA
DB8/DOUTB	25	DOUTB	DOUTB[2]	Unused
DB9/DOUTC	27	N/A	DOUTC[3]	Unused
DB10/ DOUTD	28		DOUTD[3]	Unused
DB11/SDI	29		Unused	SDI
DB12 to DB14	30 to 32		N/A	
DB15	33			

1. N/A indicates not applicable. Connect all N/A pins to AGND.
2. Used only when 2SDO or 4SDO mode is selected via the CONFIG register, otherwise leave unconnected.
3. Used only when 4SDO mode is selected via the CONFIG register, otherwise leave unconnected.

9.3 Parallel Interface

ADC data or read / write register contents through the parallel interface , tie the PAR/SER SEL pin low.

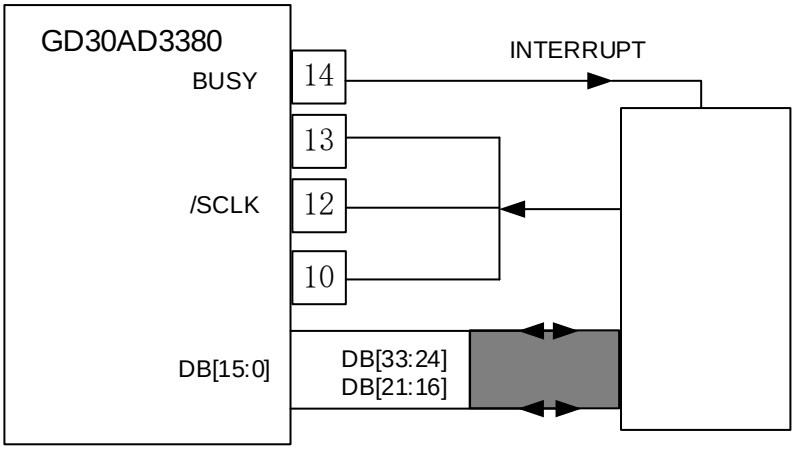


Figure 74. GD30AD3380 Interface Diagram - a GD30AD3380 Using Parallel Bus $\overline{CS}$ and $\overline{RD}$ Shorted Together

$\overline{CS}$ The rising edge of the input signal puts the bus into tri-state, and $\overline{CS}$ the falling edge of the input signal takes the bus out of high impedance state. $\overline{CS}$ It is the control signal to enable the data line. This function can allow multiple GD30AD3380 to share the same parallel data bus.

Reading conversion results (parallel ADC mode)

$\overline{RD}$ The falling edge of the pin is used to read data from the output conversion result register. A series of $\overline{RD}$ pulses are applied to $\overline{RD}$ the pin to output the conversion results from each channel to the parallel bus [DB15:DB0] in ascending order from V1 to V8 , as shown in Figure 75.

$\overline{CS}$ The signal can be permanently tied to a low level, $\overline{RD}$ the BUSY signal can access the conversion results, as shown in Figure 2. When the BUSY signal goes low, you can start reading new data (see 6.1). Alternatively, when the BUSY pin is high, you can read the data generated by the previous conversion process.

GD30AD3380 in the system and it does not share a parallel bus, the data can be read using a control signal from the digital host. $\overline{CS}$ the $\overline{RD}$ and $\overline{RD}$ signals can be connected together as shown in Figure 3. In this case, $\overline{CS}$ The falling edge of the signal takes the data bus out of tri-state and outputs the data .

FRSTDATA output signal indicates when the first channel, V1 , is being read back , as shown in Figure 3. When $\overline{CS}$ the input is high, the FRSTDATA output pin is in three-state. $\overline{CS}$ A falling edge takes the FRSTDATA pin out of three-state. The falling edge of the signal corresponding to the result for V1 $\overline{RD}$ sets the FRSTDATA pin high, indicating that the result for V1 is available on the output data bus. $\overline{RD}$ After the next falling edge of , the FRSTDATA pin returns to a logic low state.

Read during conversion

The GD30AD3380 when the BUSY pin is high and a conversion is in progress . This operation has little impact on the performance of the converter and allows for faster throughput. Data can be read from the GD30AD3380 at any time except on the falling edge of the BUSY signal, when the output data register is updated with new conversion data. Data read operations performed while the BUSY signal is high must be completed before the falling edge of the BUSY signal.

Parallel ADC mode with CRC enabled

In software mode, the parallel interface supports reading ADC data and appending a CRC when enabled by the INT_CRC_ERR_EN bit (Address 0x21 Bit 2) . The CRC is 16 bits and is output after all 8 channel conversion results are read, as shown in the following figure. The CRC calculation includes all data on the DBx pins: data, status (if appended), and zeros. For more information on CRC , see the Diagnostics section .

Enable parallel ADC mode of the status register

In software mode, setting bit 6 of the CONFIG register (address 0x02 bit 6) enables the 8 -bit status header (see Table 16), so that each channel will have two frames of data:

- The first frame outputs ADC data through DBx normally.
- The second frame outputs the status header of the channel through DB15 to DB8, with DB15 as the MSB, DB8 as the LSB, and the DB7 to DB0 pins outputting zeros.

The sequence is shown in Figure 76. Table 16 explains the status header content and each bit.

Table 15. Decoding of CH.ID Bits in the Status Header

CH.ID2	CH.ID1	CH.ID0	CHANNEL NUMBER
0	0	0	Channel 1 (V1)
0	0	1	Channel 2 (V2)
0	1	0	Channel 3 (V3)
0	1	1	Channel 4 (V4)
1	0	0	Channel 5 (V5)
1	0	1	Channel 6 (V6)
1	1	0	Channel 7 (V7)
1	1	1	Channel 8 (V8)

Table 16. Status Header, Parallel Interface

DETAILS	Bit 7 (MSB)	Position 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Bit Name	RESET_DETECT	DIGITAL_ERROR	OPEN_DETECTED	AIN_OV_DIAG_ERR	AIN_UV_DIAG_ERR	CH.ID2	CH.ID1	CH.ID0
Bit Description[1]	Reset detected	Error flag at address 0x22	The analog input of this channel is open circuit	Detected on this channel Overpressure	Detected on this channel Undervoltage	Channel ID (see Table 15 Table 15)		

1. See the Diagnosis section for more information.

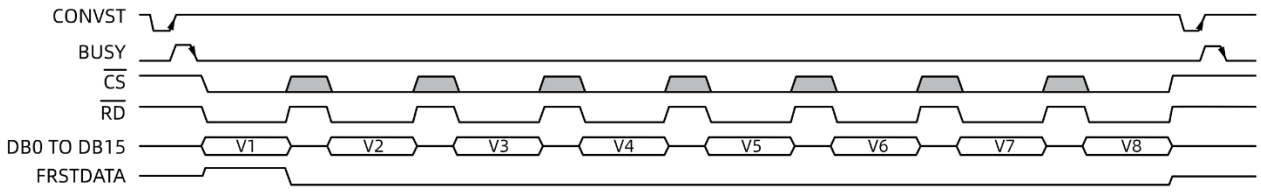


Figure 75. Parallel Interface, ADC Read Mode

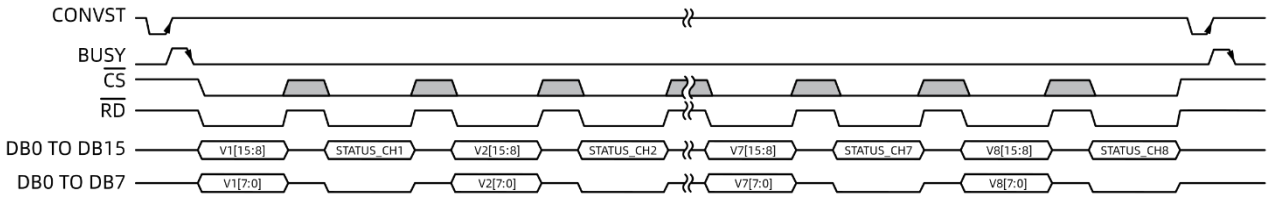


Figure 76. Parallel Interface, ADC Read Mode, Enable Status Header

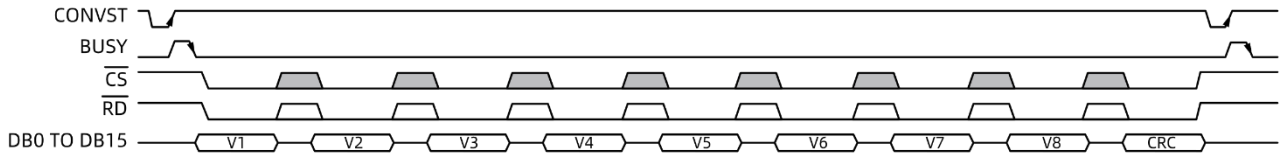


Figure 77. Parallel Interface, ADC Read Mode, CRC Enabled

Parallel Register Mode (Read Register Data)

In software mode, Register Summarya high-impedance state when both the signal and $\overline{RD}$ the signal are logic low to read the register contents, or when both $\overline{CS}$ the signal and $\overline{WR}$ the signal are logic low to write the register address and/or register contents .

Register reads are performed in two frames: first the read command is sent to the ADC , and second the ADC outputs the register contents. The format of the register read command is shown in Figure 78. In the first frame:

- Bit DB15 must be set to 1 to select the read command. The read command places the ADC in register mode.
- Bits DB[14:8] must contain the register address.
- The following 8 bits DB[7:0] are ignored.

The register address is latched on $\overline{WR}$ the GD30AD3380-I10 on the rising edge of the signal . Then, by pulling $\overline{RD}$ the line low in the next frame, the register content can be read from the latched register, as shown below:

- Pull the DB15 bit to 0.
- Bits DB[14:8] provide the register address to be read.
- The following 8 bits DB[7:0] provide the register contents.

To return to ADC read mode, write to address 0x00 as described in the Parallel Register Mode (Write Register Data) section . ADC data cannot be read while the device is in register mode .

Parallel Register Mode (Write Register Data)

In software mode, all Register Summarycan be written through the parallel interface. To write a series of registers, exit the ADC read mode (default mode) by reading any register on the memory map. Register write commands are executed in a single frame using the parallel bus (DB[15:0]) , $\overline{CS}$ signal, and $\overline{WR}$ signal. The format of the write command is shown in Figure 78. The structure of the write command format shown is as follows:

- To select a write command, Bit DB15 must be set to 0.
- Bits DB[14:8] contain the register address.
- The following 8 bits DB[7:0] contain the data to be written to the selected register.

Data $\overline{WR}$ is latched into the device on the rising edge of the pin. To return to ADC read mode, write to address 0x00. ADC data cannot be read while the device is in register mode .

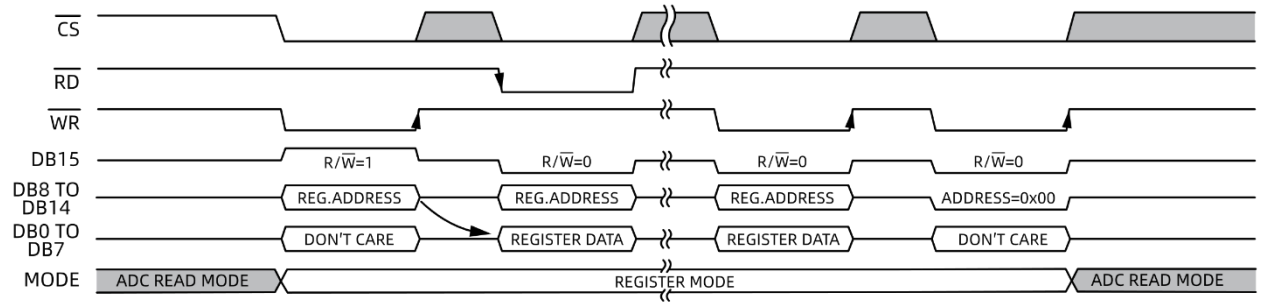


Figure 78. Parallel Interface Register Read Operation, Followed by Write Operation

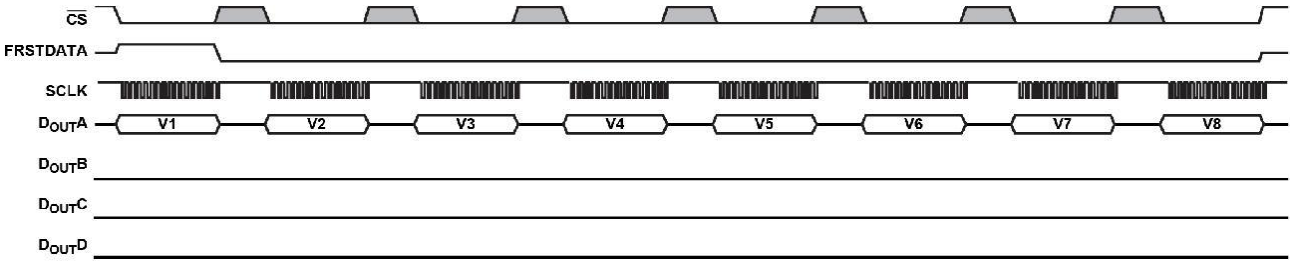


Figure 79. Serial Interface ADC Read, One D $_{OUT}$ x Line

9.4 Serial Interface

ADC data or read / write register contents through the serial interface , tie the $\overline{PAR}$ / SER SEL pin high.

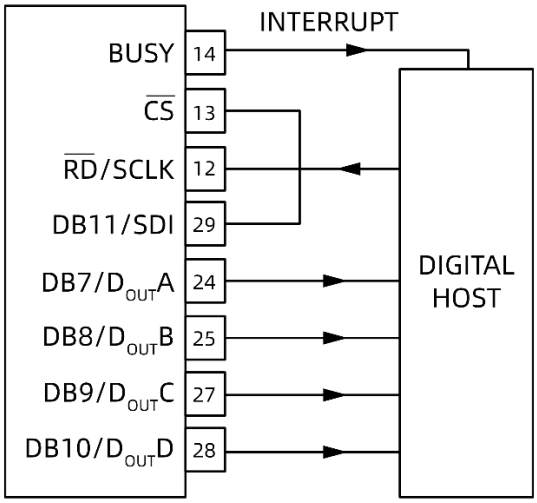


Figure 80. GD30AD3380 Interface Diagram - One GD30AD3380 using the serial interface and four DOUTX lines

Reading conversion results (serial ADC mode)

The GD30AD3380 has four serial data output pins: DOUTA , DOUTB , DOUTC , and DOUTD . In software mode, data can be read back from the GD30AD3380 using one (see Figure 80) , two (see Figure 81), or four DOUTX lines (see Figure 82), depending on the configuration set in the CONFIG register.

Table 17. DOUTX Format Selection Using the CONFIG Register (Address 0x02)

DOUTX FORMAT	ADDRESS 0x02, BIT 4	ADDRESS 0x02, BIT 3
1 DOUTX	0	0
2 DOUTX	0	1
4 DOUTX	1	0
1 DOUTX	1	1

In hardware mode, only two $D_{OUT}X$ lines can be selected. However, all channels can be read from $D_{OUT}A$ by providing eight 16-bit SPI frames between two CONVST pulses .

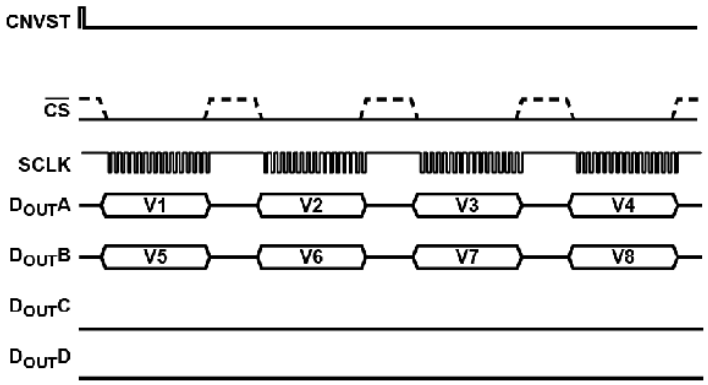


Figure 81. Serial interface ADC read, two DOUTx lines

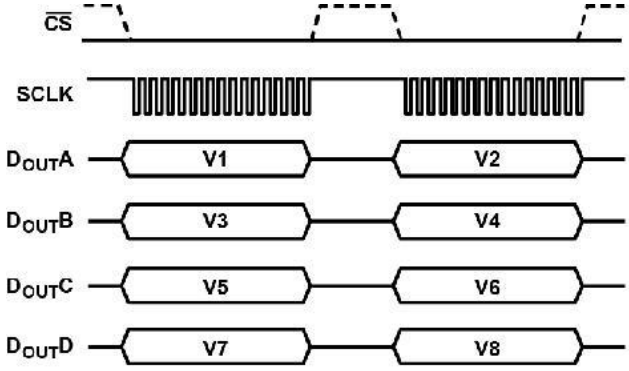


Figure 82. Serial Interface ADC Read, Four $D_{OUT}X$ Lines

$\overline{CS}$ the falling edge takes the data output lines $D_{OUT}A$ to $D_{OUT}D$ out of three-state and outputs the MSB of the conversion result .

In 3-wire mode (Figure 5, The falling edge of the $\overline{CS}$ BUSY signal outputs the MSB instead $\overline{CS}$ of the MSB . The rising edge of the SCLK signal outputs all subsequent data bits through the serial data outputs $D_{OUT}A$ through $D_{OUT}D$, as shown below. $\overline{CS}$ The input can be held low during the entire serial read operation or pulsed to provide 16 SCLK cycles for each channel read frame (see Figure 81). However, if a pulse is sent to the SCLK during the transmission of a channel conversion result $\overline{CS}$, the interrupted channel is retransmitted in the next frame, starting again with the MSB .

It is also possible to use only the $D_{OUT}A$ pin to output data, as shown in Figure 79. In order for the GD30AD3380 to access all eight conversion results through one $D_{OUT}x$ line, a total of 128 SCLK cycles are required. In hardware mode, these 128 SCLK cycles must $\overline{CS}$ be framed by the signal in groups of 16 SCLK cycles. The disadvantage of using only one $D_{OUT}X$ line is that the throughput rate is reduced if reading is performed after the conversion. In serial mode, the unused $D_{OUT}X$ lines remain unconnected.

Figure 82 shows the use of four $D_{OUT}X$ lines on the GD30AD3380 to read eight simultaneous conversion results, which can be used in software mode. In this case, 32 SCLK transmissions access data in $\overline{CS}$ the GD30AD3380 , either held low to build a full 32 SCLK cycle frame, or pulsed between two 16-bit frames. This mode is only available in software mode and is configured through the CONFIG register (Address 0x02).

Figure 5shows the timing diagram for reading data from one channel of the GD30AD3380 in serial mode ($\overline{CS}$ framed by the signal enable). The SCLK input signal provides the clock source for the serial read operation. $\overline{CS}$ the signal goes low to access the data of GD30AD3380.

FRSTDATA output signal indicates when the first channel, V1 , is being read back . When $\overline{CS}$ the input is high, the FRSTDATA output pin is tri-stated. In serial mode, $\overline{CS}$ the falling edge of the signal takes the FRSTDATA pin out of tri-state and sets the FRSTDATA pin high if the BUSY line has been deasserted .

Indicates that the result of V1 is available on the DOUTA output data line. After the 16th SCLK falling edge , the FRSTDATA output returns to a logic low state. If $\overline{CS}$ the pin is permanently tied low (3-wire mode), the falling edge of the BUSY line sets the FRSTDATA pin high when the result of V1 is available on DOUTA .

If SDI is tied low or high, nothing is input to the GD30AD3380 . Therefore, the device continues to output conversion results. When using the GD30AD3380 in 3-wire mode , SDI should be kept high. In ADC read mode, a single write operation can be performed, as shown in Figure 83. To write to a series of registers, switch to register mode, as described in the " Serial Register Mode (Writing Register Data) " section.

Read during conversion

The GD30AD3380 when the BUSY signal is high and a conversion is in progress. This operation has little impact on the performance of the converter and can achieve a faster throughput rate. Data can be read from the GD30AD3380 at any time except on the falling edge of the BUSY signal, when the output data register is updated with new conversion data. Data read operations performed while the BUSY signal is high must be completed before the falling edge of the BUSY signal.

Serial ADC mode, CRC enabled

In software mode, CRC can be enabled by writing to the register map. In this case, the CRC is appended to each DOUTX line after the last channel has finished outputting, as shown in Figure 89. For more information on how the CRC is calculated, see the Interface CRC Checksum section .

Serial ADC mode, enabled state

In software mode, when using the serial interface, an 8-bit status header can be enabled and appended after each 16- bit data conversion result, extending the frame size to 24 bits for each channel, as shown in Figure 83.

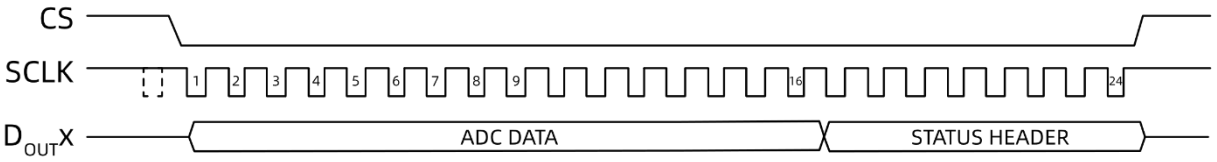


Figure 83. Serial Interface, ADC Mode, Status On

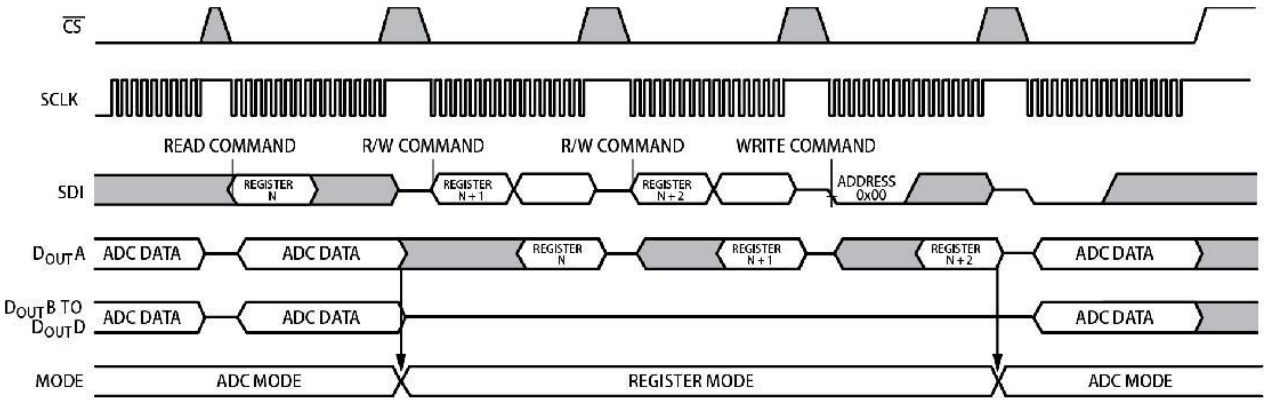


Figure 84. GD30AD3380 Register Mode

Table 18. Status Header, Serial Interface

Details	Bit 7 (MSB)	Position 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Bit Name	RESET_DETECT	DIGITAL_ERROR	OPEN_DETECTED	AIN_OV_DIAG_ERR	AIN_UV_DIAG_ERR	CH.ID2	CH.ID1	CH.ID0
Bit Description [1]	Reset detected	Error flag at address 0x22	At least one analog input on the channel is open	Overvoltage detected on channel	Undervoltage detected on channel	Channel ID (see 0)		

1. the Diagnosis section for more information.

Serial register mode (read register data)

Register Summaryis shown in Figure 45. It consists of two 16-bit frames. In the first frame:

- The first bit in SDI must be set to 0 to enable writing of the address.

- The second bit must be set to 1 to select a read command.
- Bits[3:8] in SDI contain the register address to be output on DOUTA in the next frame.
- The following 8 bits in SDI (bits [9:16]) are ignored.

If the GD30AD3380 is in ADC mode, SDO will continue to output ADC data through bits [9:16], and then the GD30AD3380 switches to register mode.

If the GD30AD3380 is in register mode, SDO will read back the contents from the previously addressed register regardless of whether the previous frame was a read or write command. To exit register mode, address 0x00 needs to be written, as shown in Figure 84.

Serial Register Mode (Write Register Data)

In software mode, Register Summarycan be written through the serial interface. To write a series of registers, exit the ADC read mode (default mode) by reading any register on the memory map. Register write commands are executed through a single 16-bit SPI read operation. The format of the write command is shown in Figure 86.

- To enable a write command, the first bit in SDI must be set to 0.
- The second (R/W) bit must be cleared to 0.
- Bits[ADD5:ADD0] contain the register address to be written.
- The next 8 bits (Bits[DIN7:DIN0]) contain the data to be written to the selected register. Data is input on SDI on the falling edge of SCLK and output on DOUTA on the rising edge of SCLK.

When writing to the device continuously, the data that appears on DOUTA is from the register address written in the previous frame, as shown in Figure 86. The DOUTB, DOUTC, and DOUTD pins remain low during the transfer.

ADC data output in register mode because the DOUTX line is used to output the register contents. After writing all required registers, writing address 0x00 returns the GD30AD3380 to ADC read mode, at which point the ADC data is again output on the DOUTX line, as shown in Figure 84.

In software mode, when CRC is turned on, 8 more bits are input and output per frame , so a 24-bit frame is required.

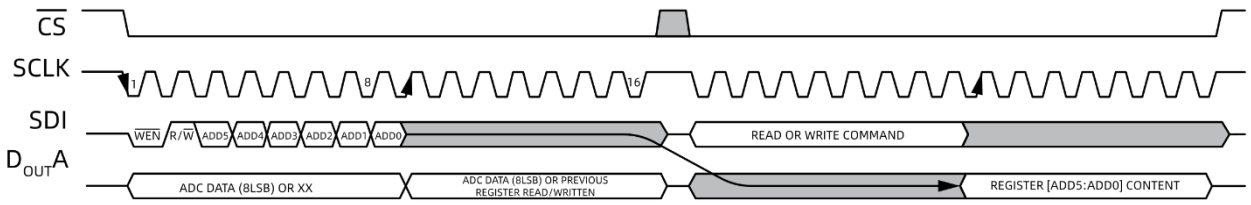


Figure 85. Serial Interface Read Command; First Frame Points to Address; Second Frame Provides Register Contents

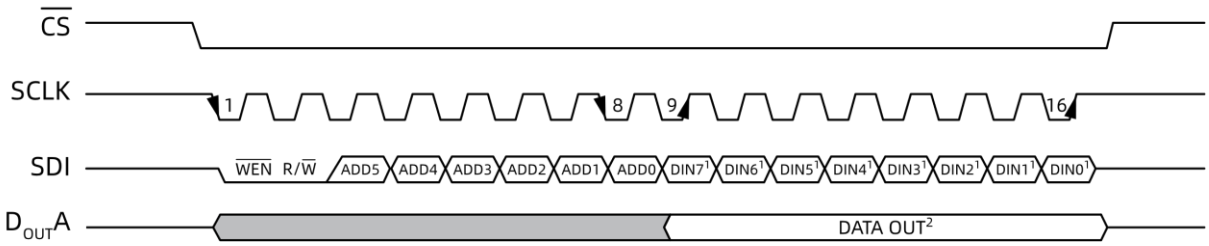


Figure 86. Serial Interface, Single Write Command; SDI Inputs the Address [ADD5:ADD0] and Register Contents [DINx] in the Same Frame, and DOUTA Provides the Register Contents Requested in the Previous Frame

Serial Register Mode Using CRC

In software mode, the registers can be written to and read from the GD30AD3380 with CRC enabled by setting the INT_CRC_ERR_EN bit (Address 0x21 Bit 2).

When reading the registers, the GD30AD3380 provides 8 additional bits on the DOUTA pin, the CRC, generated from the previously shifted out data on the same frame. The controller can then check if the received data is correct by applying the following polynomial:

$$x^8 + x^2 + x + 1 \quad (4)$$

CRC is enabled , the length of the SPI frame is extended to 24 bits, as shown in Figure 87.

When writing to a register, the controller must input the data (register address plus register contents) into the GD30AD3380, followed by an 8-bit CRC word calculated from the previous 16 bits of data using the aforementioned polynomial . The GD30AD3380 reads the register address and register contents, calculates the corresponding 8-bit CRC word, and sets the INT_CRC_ERR bit (address 0x22 bit 2) if the calculated CRC word does not match the CRC word received via SDI between bits 17 and 24, as shown in Figure 88.

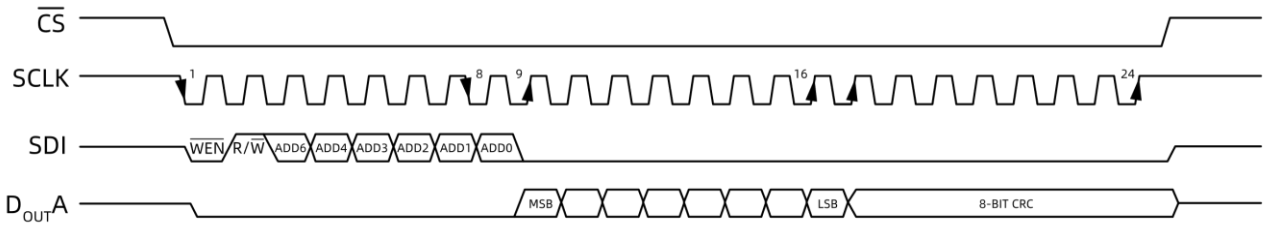


Figure 87. SPI Interface, CRC Enabled

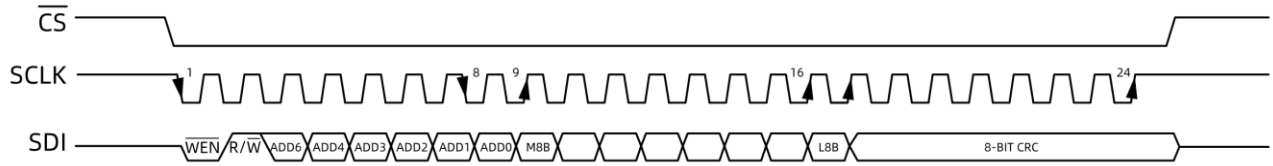


Figure 88. SPI Interface, CRC Enabled

10 diagnosis

Diagnostic features can be used in software mode to verify the correct operation of the GD30AD3380. The diagnostic monitoring list includes reset detection, overvoltage detection, undervoltage detection, analog input open circuit detection, and digital error detection.

If an error is detected, the corresponding flag is set on the status header (if enabled), as described in the *Digital* Interfacesection. The flag points to the register where the error is located, as described in the following section.

Additionally, the diagnostic multiplexer can use any channel to verify a range of internal nodes, as described in the *Diagnostic Multiplexer* section.

10.1 Reset detection

If a partial reset or full reset pulse is applied to the GD30AD3380, the RESET_DETECT bit of the status register (Address 0x01 Bit 7) is set. A full reset is required at power-up. This reset sets the RESET_DETECT bit, indicating that the power-on reset (POR) of the device has been properly initialized.

The POR monitors the REGCAP voltage and if the voltage drops below a certain threshold, a full reset occurs.

The RESET_DETECT bit can be used to detect an unexpected device reset or a large glitch on the RESET pin, or to detect a voltage drop in the power supply.

The RESET_DETECT bit can only be cleared to 0 by reading the status register .

10.2 Interface CRC Checksum

The GD30AD3380 has a CRC checksum mode that can be used to detect errors in data transmission, thereby improving the robustness of the interface. The CRC feature is available in both ADC modes (serial and parallel) and register mode (serial only).

The GD30AD3380 uses the following 8 -bit CRC polynomial to calculate the CRC checksum value:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^{8} + x^{6} + x^{4} + x^{3} + x + 1$$

To replicate the polynomial division in hardware, the data is shifted left 16 bits to produce a number ending with 16 logic 0s . The polynomial is aligned so that the MSB is adjacent to the leftmost logic 1 of the data . An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is aligned again so that the MSB is adjacent to the leftmost logic 1 of the new result , and the process is repeated. Finally, the original data is reduced to a value less than the polynomial, which is the 16 -bit checksum.

Table 19 gives an example of CRC calculation for 16-bit data. Using the above polynomial, the CRC corresponding to the data 0x064E is 0x2137 .

CRC when enabled via the INT_CRC_ERR_EN bit (Address 0x21, Bit 2) . The CRC is a 16-bit word that is appended to the end of each $D_{OUT}X$ used after all channels have been read . An example using four $D_{OUT}X$ lines is shown in Figure 89.

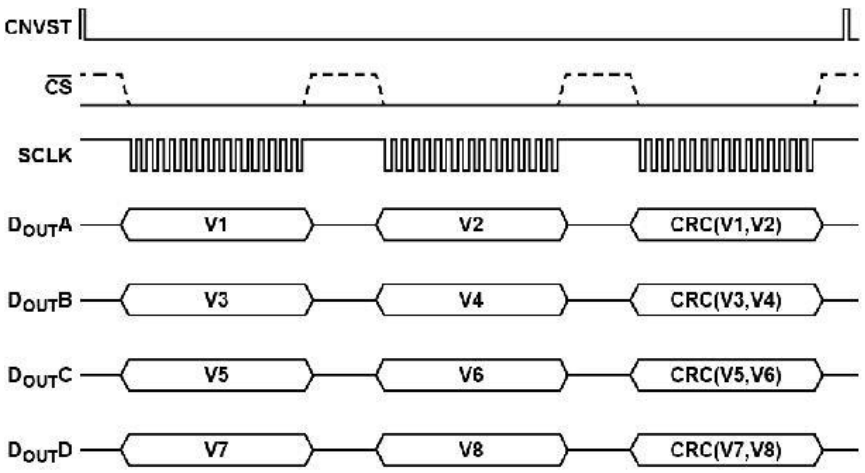


Figure 89Serial Interface ADC Read, CRC On, Four D OUT x Lines

If two $D_{OUT}X$ lines are used ($D_{OUT}A$ and $D_{OUT}B$), each 16- bit CRC word is calculated Figure 90 using data from four channels (that is, 64 bits), as shown in Figure 50. If only one $D_{OUT}X$ line is used, all eight channels are output through $D_{OUT}A$, followed by a 16-bit CRC word calculated using data from eight channels (that is, 128 bits).

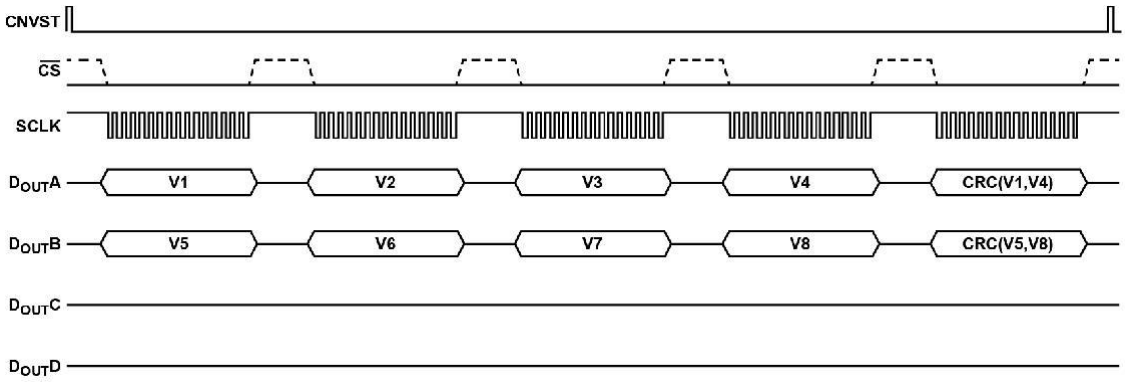


Figure 90. Serial Interface ADC Read, CRC On, Two $D_{OUT}X$ Lines

When the GD30AD3380 is in register mode, that is, when reading or writing registers, the CRC polynomial used is x^8+x^2+x+1. When reading registers and enabling CRC, each SPI frame length is 24 bits, and the CRC 8 -bit word is output on the 17th to 24th SCLK cycle. Similarly, when writing registers, a CRC word can be appended to the SDI line , as shown by 0; if the given CRC does not match the internally calculated value, the GD30AD3380 will check and trigger the error INT_CRC_ERR (address 0x22 bit 2).

CRC in ADC mode only and is output through DB15 to DB0 after channel 8 , as shown in Figure 77. The 16-bit CRC word is calculated using data from 8 channels, or 128 bits.

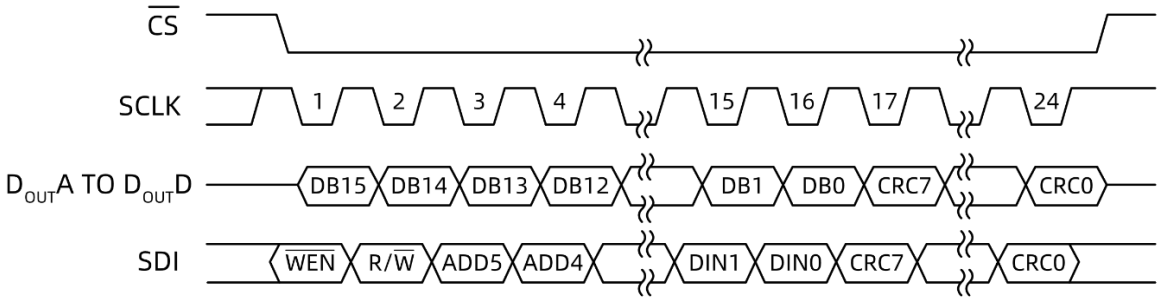


Figure 91. CRC Enabled

Table 19. for bit data[1]

Data[2]	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Process data	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Polynomial						1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1										
						0	1	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	0									
							1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1									
							0	1	0	1	1	1	0	0	0	1	1	1	0	1	1	0	1	0								
								1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1								
								0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0		
														1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1		
														0	0	1	0	1	0	1	0	1	0	0	0	1	1	0	1	1	0	0
																1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1
CRC																	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1

1. This table represents the division of data. Blank cells are used for formatting.
2. X = don’t care.

Interface Check

By setting the INTERFACE_CHECK_EN bit (Address 0x21 , Bit 7). Selecting the interface check forces the conversion result registers to known values, as shown in Table 20.

Verify that the controller receives Table 20 that the interface between the GD30AD3380 and the controller is functioning properly. If the interface CRC is enabled because the data being transmitted is known, this mode verifies that the controller performs the CRC calculation correctly.

Table 20. Interface check conversion results

CHANNEL NUMBER	FORCE CONVERSION RESULT(HEXADECIMAL)
V1	0xACCA
V2	0x5CC5
V3	0xA33A
V4	0x5335
V5	0xCAAC
V6	0xC55C
V7	0x3AA3
V8	0x3553

SPI invalid read/write

When an attempt is made to read back an invalid register address, the SPI_READ_ERR bit (Address 0x22 , Bit 4) is set . Invalid readback address detection can be enabled by setting the SPI_READ_ERR_EN bit (Address 0x21, Bit 4). If an SPI read error is triggered, it can be cleared by overwriting this bit or disabling the check function.

When an attempt is made to write to an invalid register address or a read-only register, the SPI_WRITE_ERR bit (Address 0x22, Bit 3) is set . Invalid write address detection can be enabled by setting the SPI_WRITE_ERR bit (Address 0x21, Bit 3). If an SPI write error is triggered, it can be cleared by overwriting this bit or disabling the check function.

BUSY blocking high level

BUSY stuck high level monitoring can be enabled by setting the BUSY_STUCK_HIGH_ERR_EN bit (Address 0x21 Bit 5) . When this bit is enabled, an independent clock is used internally to monitor the conversion time (*GD30AD3380-I10 General* Timing Specifications). If t_{CONV} exceeds 4µs , the GD30AD3380 meeting since move Enter OK department point complex Bit and Place The BUSY_STUCK_HIGH_ERR bit (Address 0x22 , Bit 5) is set to 1. To clear this error flag, the BUSY_STUCK_HIGH_ERR bit must be overwritten with 1 .

When oversampling mode is enabled, the conversion time of each internal conversion is monitored.

10.3 Diagnostic Multiplexer

All eight input channels have a diagnostic multiplexer in front of 0GD30AD3380 is operating correctly. As an example, Table 21 shows the bit decoding of the diagnostic multiplexer register on channel 1. When an internal node is selected, the input voltage of the input pin is deselected from the PGA , as shown in Figure 92.

In software mode, each diagnostic multiplexer configuration is accessed through the corresponding registers (Address 0x28 to Address 0x2B). To use the multiplexer on one channel, the ±10 V range must be selected on

that channel.

Table 21. Channel 1 Diagnostic Multiplex Register Bit Decoding

Address 0x18			
Bit 2	**Bit 1**	**Bit 0**	**Signal on channel 1**
0	0	0	V1
0	0	1	Temperature Sensor
0	1	0	V_{REF}
0	1	1	ALDO
1	0	0	DLDO
1	0	1	V_{DRIVE}
1	1	0	AGND
1	1	1	AV_{CC}

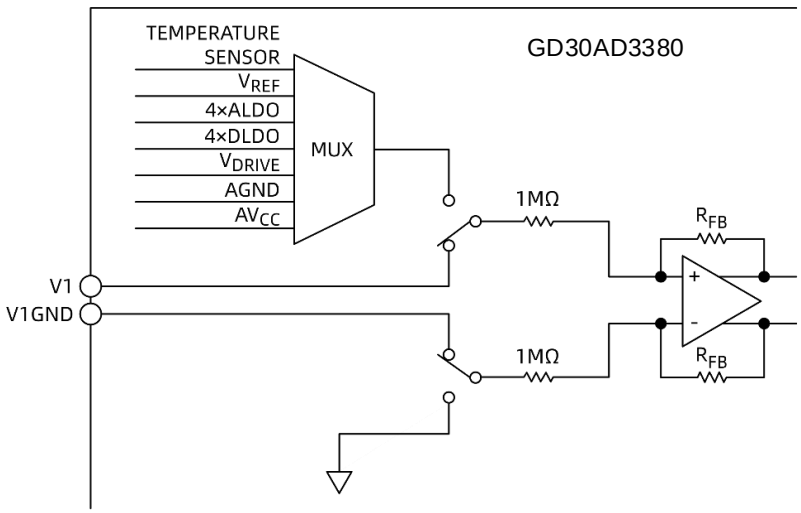


Figure 92. Diagnostic Multiplexer (Channel 1 shown as an example)

Temperature Sensor

The temperature sensor can be selected through the diagnostic multiplexer and converted by the ADC as shown in Figure 92. The temperature sensor voltage is measured and is proportional to the die temperature as shown in the following equation:

$$\text{Temperature}(^{\circ}\text{C}) = \frac{\text{ADC}_{\text{OUT}}(\text{V}) - 0.69068(\text{V})}{0.019328(\text{V}/^{\circ}\text{C})} + 25(^{\circ}\text{C}) \quad (5)$$

$$\text{Temperature}(^{\circ}\text{C}) = \frac{\text{ADC}_{\text{OUT}}(\text{V}) - 0.502(\text{V})}{1.62e^{-3}(\text{V}/^{\circ}\text{C})} + 25(^{\circ}\text{C}) \quad (6)$$

Accuracy is ±2°C .

Internal LDO

The analog and digital LDOs (REGCAP pins) can be selected through the diagnostic multiplexer and converted by the ADC as shown in Figure 92. The ADC output is four times the voltage at the REGCAPA and REGCAPD pins, respectively. This measurement verifies that each LDO is at the correct operating voltage so that the internal circuitry is properly biased.

Supply voltage

AV_{CC} , V_{DRIVE} , and AGND can be selected through the diagnostic multiplexer and converted by the ADC , as shown in Figure 92. This setup ensures that the correct voltages and grounds are applied to the device for proper operation.

Reference voltage

The reference voltage can be selected through the diagnostic multiplexer and converted by the ADC , as shown in Figure 93. Depending on the REF SELECT pin, either the internal or external reference voltage is selected as the input to the diagnostic multiplexer. Ideally, the ADC output voltage varies with the reference voltage level at a certain ratio. Therefore, if the ADC output is outside the expected 2.5 V , the reference buffer or PGA is malfunctioning.

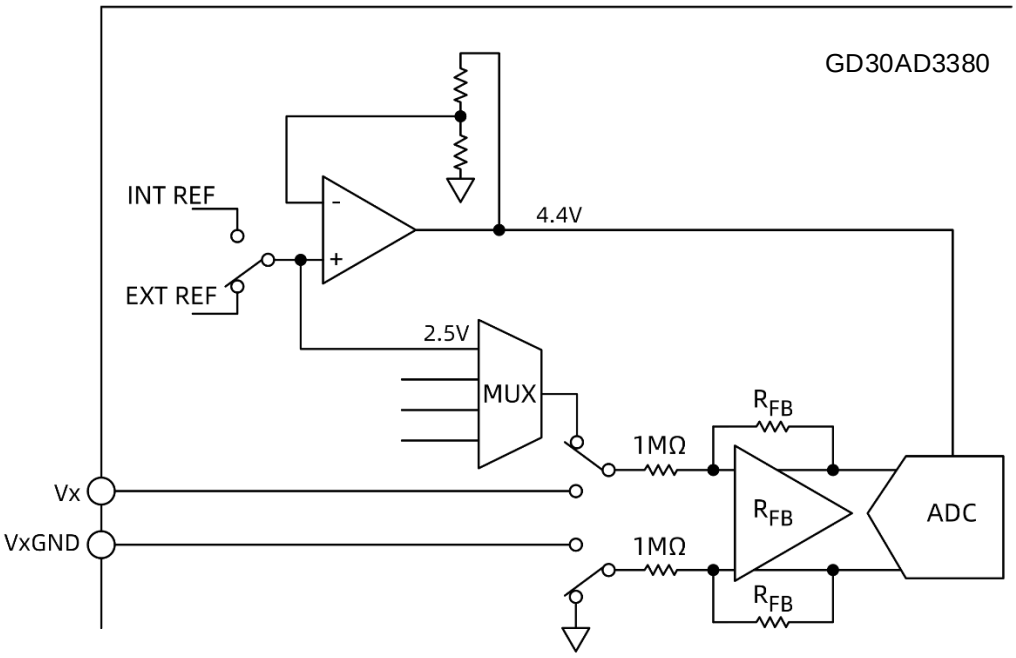


Figure 93. Reference Voltage Signal Path Through the Diagnostic Multiplexer

11 Typical connection diagram

AVCC supply pins on the device . It is recommended to use a 100 nF decoupling capacitor for each of the four supply pins and a 10 µF capacitor on the supply side. The GD30AD3380 can operate with either an internal reference voltage or an externally applied reference voltage. When only one GD30AD3380 device is on the board, the REFIN/REFOUT pins should be decoupled with a 100 nF capacitor . When multiple GD30AD3380 devices are used in an application, refer to the Reference Voltage section. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF ceramic capacitor.

The V_{DRIVE} supply connects to the same power supply as the processor. The V_{DRIVE} voltage controls the voltage value of the output logic signals. For more information on layout, decoupling, and grounding, refer to the *Layout* Guidelinessection.

Applying power to the GD30AD3380 , the GD30AD3380 should be reset to ensure it is configured in the correct operating mode.

In Figure 94, the GD30AD3380 is configured in hardware mode and operates with the internal reference voltage because the REF SELECT pin is set to logic high. In this example, the device also uses a parallel interface because the PAR/SER pin is tied to AGND . The analog input range for all eight channels is ±10V as long as the RANGE pin is tied high and the oversampling rate is controlled by the controller through the OS pin.

In Figure 95, the GD30AD3380 is configured in software mode because all three OS2 , OS1 , and OS0 pins are at logic high. The oversampling rate and range of each channel are configured by accessing the memory map. In this example, the PAR/SER pin is at logic high. Therefore, reading ADC data and reading and writing the memory map both use the serial interface. The REF SELECT pin is connected to AGND . Therefore, the internal reference voltage is disabled and the external reference voltage is connected externally to the REFIN/REFOUT pins and decoupled by a 100 nF capacitor.

Figure 94 and Figure 95 Other combinations of reference voltages, data interfaces, and operating modes are possible, depending on the logic levels applied to each configuration pin.

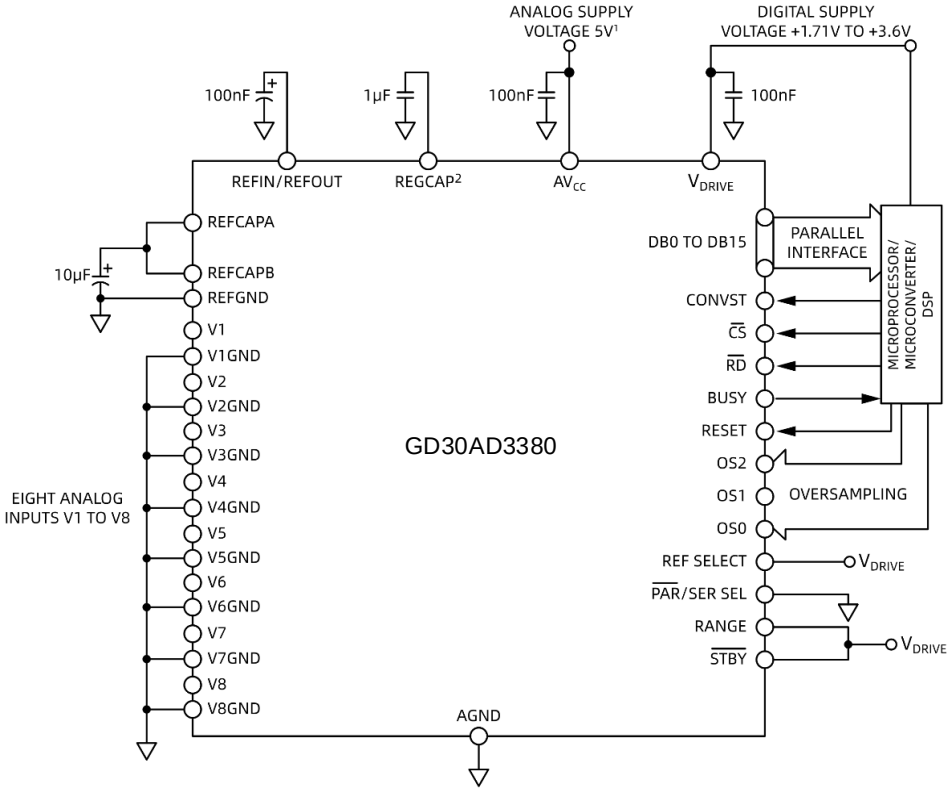


Figure 94. GD30AD3380 Typical Connection Diagram, Hardware Mode

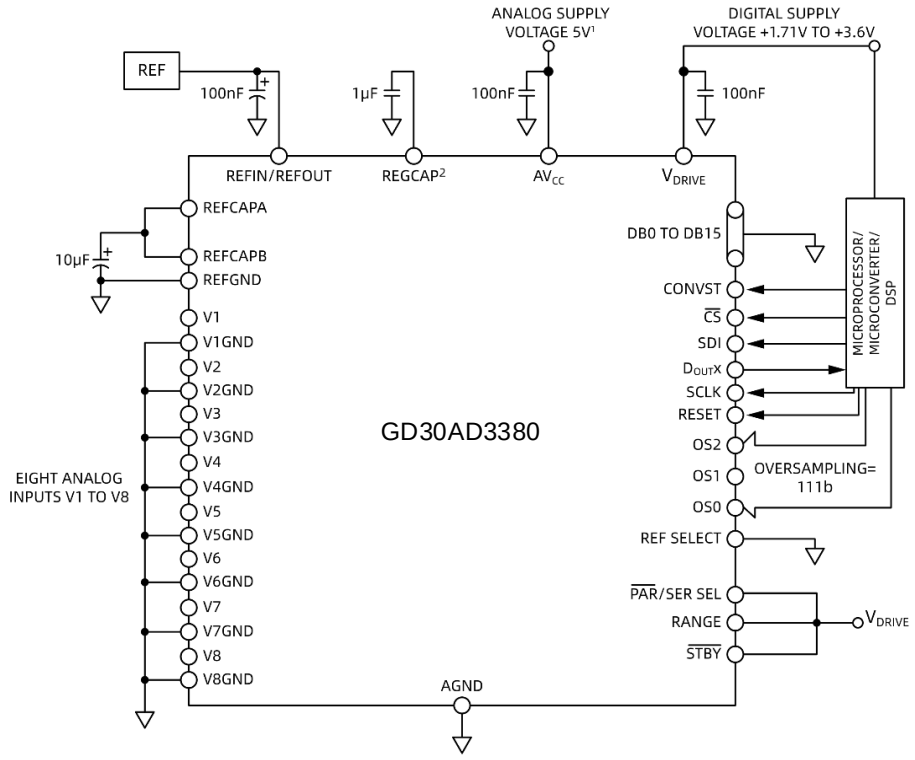


Figure 95. Typical Connection Diagram, Software Mode

12 Application Information

12.1 Layout Guidelines

When designing a PCB to mount the GD30AD3380, it is recommended to follow the following layout guidelines:

- The analog and digital sections are separated and confined to different areas of the board.
- Use at least one ground plane layer.
- If there are multiple devices in the system where the GD30AD3380 is located that require analog-to-digital grounding, single-point grounding should still be adhered to, and the grounding point should be placed as close to the GD30AD3380 as possible at a star grounding point.
- Establish a stable connection to the ground plane. Avoid situations where multiple ground pins share a common connection to the ground plane via or trace. Each ground pin should be connected to the power plane using a single via or multiple vias.
- Avoid running digital lines directly under the device as this will couple noise into the chip. Allow the analog ground plane to run under the GD30AD3380 to avoid noise coupling.
- CONVST or clock should be shielded with digital ground to avoid radiating noise to other parts of the board, and fast switching signals should never be placed close to analog signal paths.
- Avoid overlapping of digital and analog signal traces.
- Traces on adjacent layers on the board should be run perpendicular to each other to reduce feedthrough effects on the board.
- the AV_{CC} and $V_{DRIVE\ pins}$ on the GD30AD3380 should use as wide a trace as possible to provide a low impedance path and reduce the effects of glitch noise on the power lines. If possible, use a power plane and establish a stable connection between the GD30AD3380 power pins and the power traces of the circuit board. Use a single via or multiple vias for each power pin.
- The decoupling capacitors should be placed close to (ideally right next to) the power supply pins and their corresponding ground pins. The decoupling capacitors for the REFIN/REFOUT pins, REFCAPA pins, and REFCAPB pins should be placed as close as possible to their respective GD30AD3380 pins. If possible, these pins should be placed on the same side of the board as the GD30AD3380 device.

Figure 96 shows the recommended decoupling configuration for the top layer of the GD30AD3380 board. Figure 97 shows the bottom layer decoupling configuration, which is used for decoupling the four AVCC pins and the VDRIVE pin. The 100 nF ceramic capacitors for the AVCC pins are close to the corresponding pins of the device, and a 100 nF capacitor can be shared between pin 37 and pin 38 .

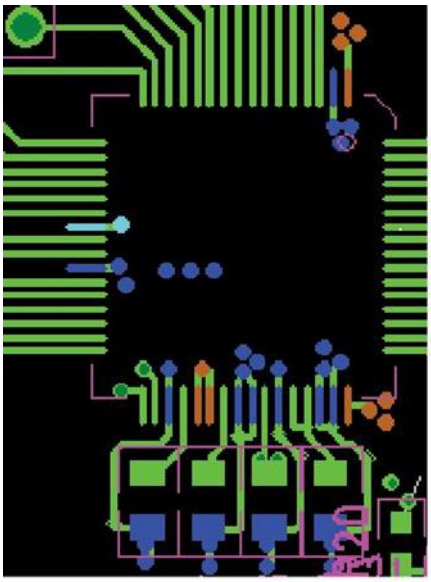


Figure 96. Top-Level Decoupling for REFIN/REFOUT, REFCAPA, REFCAPB, and REGCAP Pins

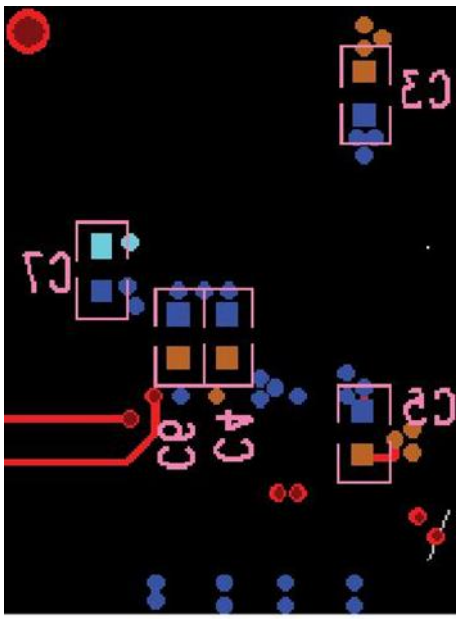


Figure 97. Layer Decoupling

In a system with multiple GD30AD3380 devices, to ensure stable performance matching between Figure 98shows the layout with two GD30AD3380 devices. The AVCC power plane is routed along the right side of the two devices, and the VDRIVE power trace is routed along the left side of the two devices. The reference voltage chip is located between the two devices, and the reference voltage trace is routed north to pin 42 of U1 and south to pin 42 of U2 . Use a solid ground plane.

These symmetrical layout principles also apply to systems with more than two GD30AD3380 devices. The GD30AD3380 devices can be placed in a north-south direction with the reference voltage in the middle of the device and the reference voltage traces running in a north-south direction, similar to Figure 98.

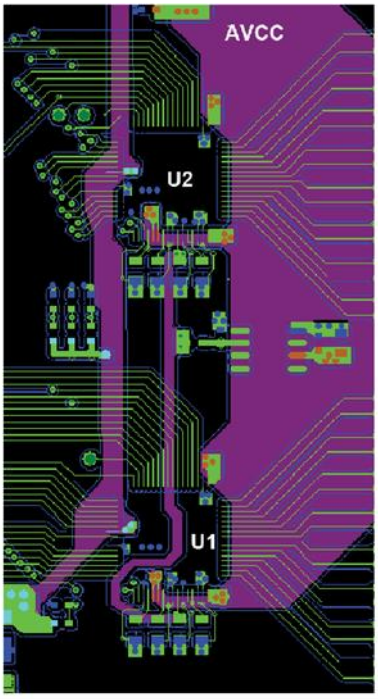


Figure 98. Multiple GD30AD3380 Devices-Top and Power Planes

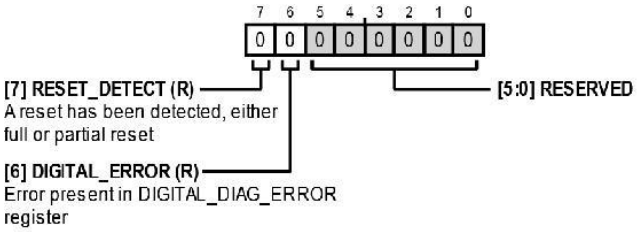
13 Register Summary

Addr	Name	Bit 7	Position 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R W
0x01	STATUS	RESET_ DETECT	DIGITAL_ ERROR	RESERVED						0x00	R
0x02	CONFIG	RESERVED	STATUS_ HEADER	EXT_OS_ CLOCK	DOUT_FORMAT		RESERVED	OPERATION_MODE		0x00	R/W
0x03	RANGE_CH1_CH2	CH2_RANGE				CH1_RANGE				0x22	R/W
0x04	RANGE_CH3_CH4	CH4_RANGE				CH3_RANGE				0x22	R/W
0x05	RANGE_CH5_CH6	CH6_RANGE				CH5_RANGE				0x22	R/W
0x06	RANGE_CH7_CH8	CH8_RANGE				CH7_RANGE				0x22	R/W
0x08	OVERSAMPLING	OS_PAD				OS_RATIO				0x00	R/W
0x09	CH1_GAIN	RESERVED		CH1_GAIN						0x00	R/W
0x0A	CH2_GAIN	RESERVED		CH2_GAIN						0x00	R/W
0x0B	CH3_GAIN	RESERVED		CH3_GAIN						0x00	R/W
0x0C	CH4_GAIN	RESERVED		CH4_GAIN						0x00	R/W
0x0D	CH5_GAIN	RESERVED		CH5_GAIN						0x00	R/W
0x0E	CH6_GAIN	RESERVED		CH6_GAIN						0x00	R/W
0x0F	CH7_GAIN	RESERVED		CH7_GAIN						0x00	R/W
0x10	CH8_GAIN	RESERVED		CH8_GAIN						0x00	R/W
0x11	CH1_OFFSET	CH1_OFFSET								0x80	R/W
0x12	CH2_OFFSET	CH2_OFFSET								0x80	R/W
0x13	CH3_OFFSET	CH3_OFFSET								0x80	R/W
0x14	CH4_OFFSET	CH4_OFFSET								0x80	R/W
0x15	CH5_OFFSET	CH5_OFFSET								0x80	R/W
0x16	CH6_OFFSET	CH6_OFFSET								0x80	R/W
0x17	CH7_OFFSET	CH7_OFFSET								0x80	R/W
0x18	CH8_OFFSET	CH8_OFFSET								0x80	R/W
0x19	CH1_PHASE	CH1_PHASE_OFFSET								0x00	R/W
0x1A	CH2_PHASE	CH2_PHASE_OFFSET								0x00	R/W
0x1B	CH3_PHASE	CH3_PHASE_OFFSET								0x00	R/W
0x1C	CH4_PHASE	CH4_PHASE_OFFSET								0x00	R/W
0x1D	CH5_PHASE	CH5_PHASE_OFFSET								0x00	R/W
0x1E	CH6_PHASE	CH6_PHASE_OFFSET								0x00	R/W
0x1F	CH7_PHASE	CH7_PHASE_OFFSET								0x00	R/W
0x20	CH8_PHASE	CH8_PHASE_OFFSET								0x00	R/W
0x21	DIGITAL_DIAG_ ENABLE	RESERVED					INT_CRC_ ERR_EN	RESERVED		0x00	R/W

Addr	Name	Bit 7	Position 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R W
0x22	DIGITAL_ DIAG_ERR	RESERVED					INT_CRC_ ERR	RESERVED		0x00	R/W
0x23	OPEN_DETECT_ ENABLE	CH8_OPEN_D ETECT_EN	CH7_OPEN_D ETECT_EN	CH6_OPEN_D ETECT_EN	CH5_OPEN_ DETECT_EN	CH4_OPE N_DETEC T_EN	CH3_OPEN_ DETECT_EN	CH2_OPEN_ DETECT_EN	CH1_OPEN_ DETECT_EN	0x00	R/W
0x24	OPEN_DETECTED	CH8_OPEN	CH7_OPEN	CH6_OPEN	CH5_OPEN	CH4_OPE N	CH3_OPEN	CH2_OPEN	CH1_OPEN	0x00	R/W
0x25	AIN_OV_UV_DIAG_ ENABLE	RESERVED								0x00	R/W
0x26	AIN_OV_DIAG_ER ROR	RESERVED								0x00	R/W
0x27	AIN_UV_DIAG_ER ROR	RESERVED								0x00	R/W
0x28	DIAGNOSTIC_MUX _CH1_2	RESERVED		CH2_DIAG_MUX_CTRL			CH1_DIAG_MUX_CTRL			0x00	R/W
0x29	DIAGNOSTIC_MUX _CH3_4	RESERVED		CH4_DIAG_MUX_CTRL			CH3_DIAG_MUX_CTRL			0x00	R/W
0x2A	DIAGNOSTIC_MUX _CH5_6	RESERVED		CH6_DIAG_MUX_CTRL			CH5_DIAG_MUX_CTRL			0x00	R/W
0x2B	DIAGNOSTIC_MUX _CH7_8	RESERVED		CH8_DIAG_MUX_CTRL			CH7_DIAG_MUX_CTRL			0x00	R/W
0x2C	OPEN_DETECT_ QUEUE	OPEN_DETECT_QUEUE								0x00	R/W
0x2D	FS_CLK_COUNTE R	CLK_FS_COUNTER								0x00	R
0x2E	OS_CLK_COUNTE R	CLK_OS_COUNTER								0x00	R
0x2F	ID	DEVICE_ID				SILICON_REVISION				0x10	R

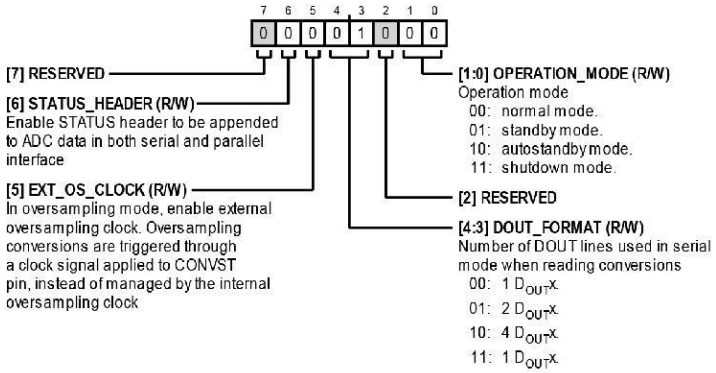
14 Register Details

Address: 0x01 ; Power-on reset: 0x00 ; Name: STATUS



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
7	RESET_DETECT	A reset has been detected, either full or partial.	0x0	R
6	DIGITAL_ERROR	There is an error in the DIGITAL_DIAG_ERROR register.	0x0	R
[5:0]	RESERVED	reserve.	0x0	R

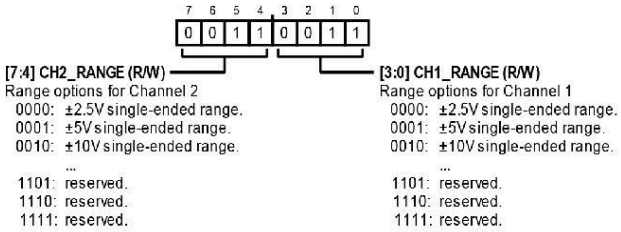
Address: 0x02 ; Reset: 0x00 ; Name: CONFIG



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
7	RESERVED	reserve.	0x0	R
6	STATUS_HEADER	Enables the STATUS header to be appended to the ADC data in the serial and parallel interfaces.	0x0	R/W
5	EXT_OS_CLOCK	In oversampling mode, an external oversampling clock is enabled. Oversampling conversions are triggered by the clock signal applied to the CONVST pin instead of being managed by the internal oversampling clock.	0x0	R/W
[4:3]	DOUT_FORMAT	$D_{OUT}X$ lines to use when reading conversion results in serial mode .	0x0	R/W
		00:1 $D_{OUT}X$.		
		01:2 $D_{OUT}X$.		
		10:4 $D_{OUT}X$.		
		11:1 $D_{OUT}X$.		

BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
2	RESERVED	reserve.	0x0	R
[1:0]	OPERATION_MODE	Working mode. 00: Normal mode. 01: Standby mode. 10: Automatic standby mode. 11: Shutdown mode.	0x0	R/W

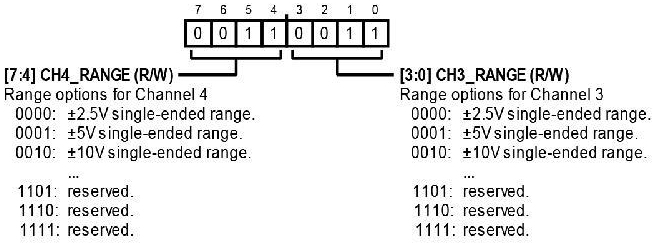
Address: 0x03 ; Reset: 0x22 ; Name: RANGE_CH1_CH2



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:4]	CH2_RANGE	Channel 2 range options. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±12.5 V single-ended range. 0100: Reserved. 0101: Reserved. 0110: Reserved. 0111: Reserved. 1000: Reserved. 1001: Reserved. 1010: Reserved. 1011: Reserved. 1100: Reserved. 1101: Reserved. 1110: Reserved. 1111: Reserved.	0x2	R/W
[3:0]	CH1_RANGE	Channel 1 range options. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±12.5 V single-ended range. 0100: Reserved.	0x2	R/W

BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
		0101: Reserved.		
		0110: Reserved.		
		0111: Reserved.		
		1000: Reserved.		
		1001: Reserved.		
		1010: Reserved.		
		1011: Reserved.		
		1100: Reserved.		
		1101: Reserved.		
		1110: Reserved.		
		1111: Reserved.		

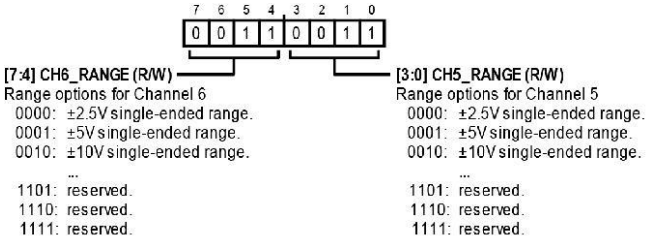
Address: 0x04 ; Reset: 0x22 ; Name: RANGE_CH3_CH4



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:4]	CH4_RANGE	Channel 4 range options.	0x2	R/W
		0000: ±2.5 V single-ended range.		
		0001: ±5 V single-ended range.		
		0010: ±10 V single-ended range.		
		0011: ±12.5 V single-ended range.		
		0100: Reserved.		
		0101: Reserved.		
		0110: Reserved.		
		0111: Reserved.		
		1000: Reserved.		
		1001: Reserved.		
		1010: Reserved.		
		1011: Reserved.		
		1100: Reserved.		
		1101: Reserved.		
		1110: Reserved.		
		1111: Reserved.		
[3:0]	CH3_RANGE	Channel 3 range options.	0x2	R/W

BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
		0000: ±2.5 V single-ended range.		
		0001: ±5 V single-ended range.		
		0010: ±10 V single-ended range.		
		0011: ±12.5 V single-ended range.		
		0100: Reserved.		
		0101: Reserved.		
		0110: Reserved.		
		0111: Reserved.		
		1000: Reserved.		
		1001: Reserved.		
		1010: Reserved.		
		1011: Reserved.		
		1100: Reserved.		
		1101: Reserved.		
		1110: Reserved.		
		1111: Reserved.		

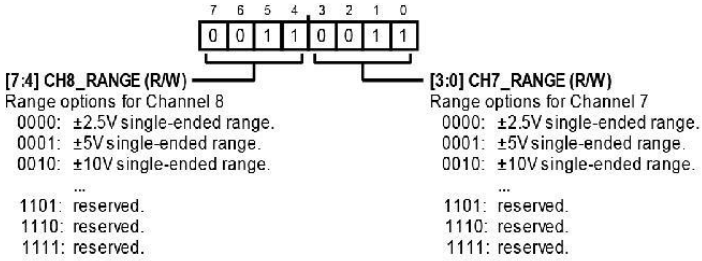
Address: 0x05 ; Reset: 0x22 ; Name: RANGE_CH5_CH6



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:4]	CH6_RANGE	Channel 6 range option.	0x2	R/W
		0000: ±2.5 V single-ended range.		
		0001: ±5 V single-ended range.		
		0010: ±10 V single-ended range.		
		0011: ±12.5 V single-ended range.		
		0100: Reserved.		
		0101: Reserved.		
		0110: Reserved.		
		0111: Reserved.		
		1000: Reserved.		
		1001: Reserved.		
		1010: Reserved.		
		1011: Reserved.		

BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
		1100: Reserved.		
		1101: Reserved.		
		1110: Reserved.		
		1111: Reserved.		
[3:0]	CH5_RANGE	Channel 5 range options.	0x2	R/W
		0000: ±2.5 V single-ended range.		
		0001: ±5 V single-ended range.		
		0010: ±10 V single-ended range.		
		0011: ±12.5 V single-ended range.		
		0100: Reserved.		
		0101: Reserved.		
		0110: Reserved.		
		0111: Reserved.		
		1000: Reserved.		
		1001: Reserved.		
		1010: Reserved.		
		1011: Reserved.		
		1100: Reserved.		
		1101: Reserved.		
		1110: Reserved.		
		1111: Reserved.		

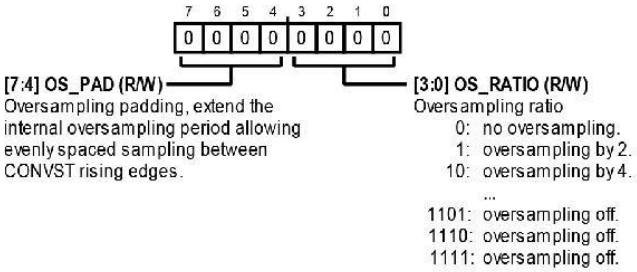
Address: 0x06 ; Reset: 0x22 ; Name: RANGE_CH7_CH8



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:4]	CH8_RANGE	Channel 8 range option.	0x2	R/W
		0000: ±2.5 V single-ended range.		
		0001: ±5 V single-ended range.		
		0010: ±10 V single-ended range.		
		0011: ±12.5 V single-ended range.		
		0100: Reserved.		
		0101: Reserved.		
		0110: Reserved.		

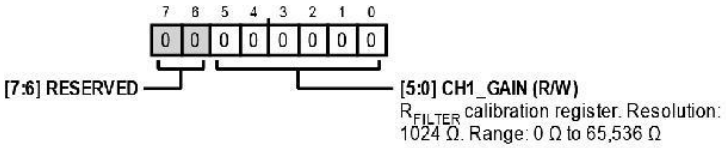
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
		0111: Reserved.		
		1000: Reserved.		
		1001: Reserved.		
		1010: Reserved.		
		1011: Reserved.		
		1100: Reserved.		
		1101: Reserved.		
		1110: Reserved.		
		1111: Reserved.		
[3:0]	CH7_RANGE	Channel 7 range options.	0x2	R/W
		0000: ±2.5 V single-ended range.		
		0001: ±5 V single-ended range.		
		0010: ±10 V single-ended range.		
		0011: ±12.5 V single-ended range.		
		0100: Reserved.		
		0101: Reserved.		
		0110: Reserved.		
		0111: Reserved.		
		1000: Reserved.		
		1001: Reserved.		
		1010: Reserved.		
		1011: Reserved.		
		1100: Reserved.		
		1101: Reserved.		
		1110: Reserved.		
		1111: Reserved.		

Address: 0x08 ; Reset: 0x00 ; Name: OVERSAMPLING



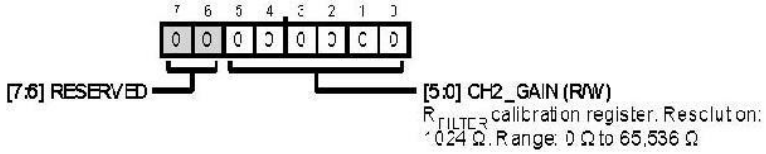
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:4]	OS_PAD	Oversampling fill, which extends the internal oversampling period, allowing samples to be evenly spaced between CONVST rising edges.	0x0	R/W
[3:0]	OS_RATIO	Oversampling ratio. 0: No oversampling. 1: 2 times oversampling. 10: 4x oversampling. 11: 8x oversampling. 100: 16x oversampling. 101: 32 times oversampling. 110: 64 times oversampling. 111: 128 times oversampling. 1000: 256 times oversampling. 1001: Oversampling off. 1010: Oversampling off. 1011: Oversampling off. 1100: Oversampling off. 1101: Oversampling is off. 1110: Oversampling off. 1111: Oversampling is off.	0x0	R/W

Address: 0x09 ; Reset: 0x00 ; Name: CH1_GAIN



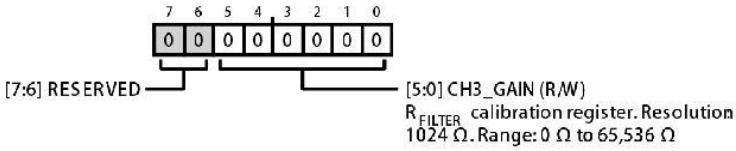
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH1_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0A ; Reset: 0x00 ; Name: CH2_GAIN



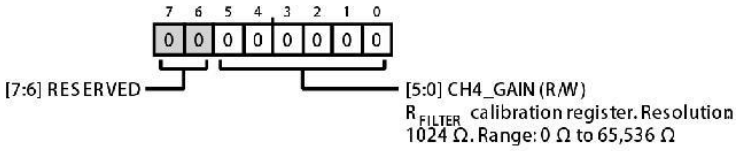
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH2_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0B ; Reset: 0x00 ; Name: CH3_GAIN



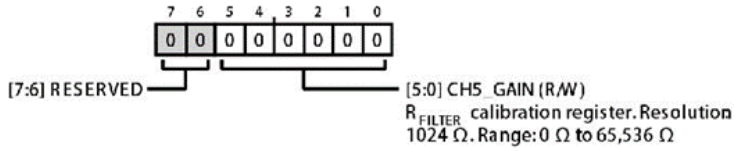
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH3_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0C ; Reset: 0x00 ; Name: CH4_GAIN



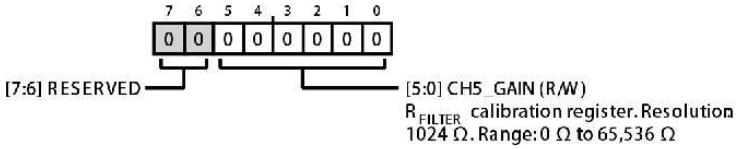
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH4_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0D ; Reset: 0x00 ; Name: CH5_GAIN



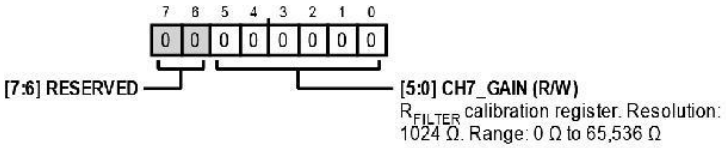
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH5_GAIN	R FILTER calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0E ; Reset: 0x00 ; Name: CH6_GAIN



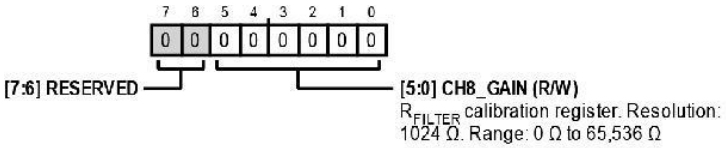
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH6_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0F ; Reset: 0x00 ; Name: CH7_GAIN



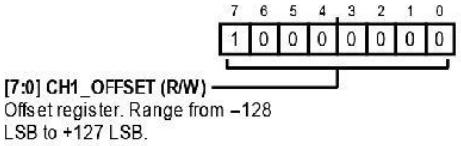
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH7_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x10 ; Reset: 0x00 ; Name: CH8_GAIN



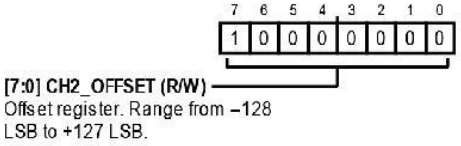
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:0]	CH8_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x11 ; Reset: 0x80 ; Name: CH1_OFFSET



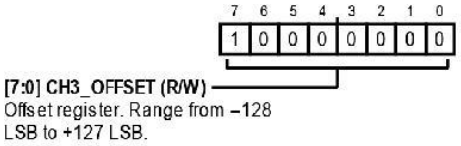
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH1_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x12; Reset: 0x80; Name: CH2_OFFSET



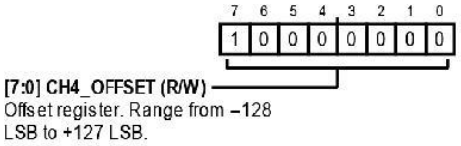
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH2_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x13 ; Reset: 0x80 ; Name: CH3_OFFSET



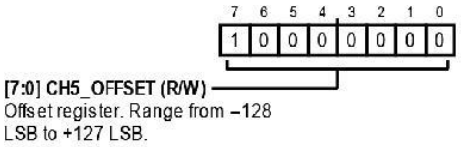
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH3_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x14 ; Reset: 0x80 ; Name: CH4_OFFSET



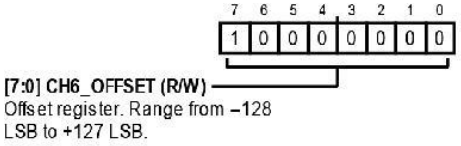
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH4_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x15 ; Reset: 0x80 ; Name: CH5_OFFSET



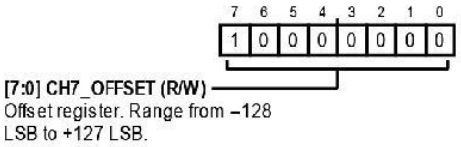
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH5_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x16 ; Reset: 0x80 ; Name: CH6_OFFSET



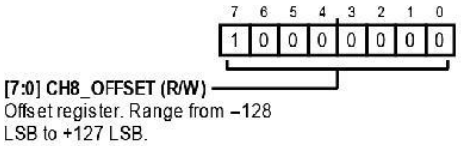
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH6_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x17 ; Reset: 0x80 ; Name: CH7_OFFSET



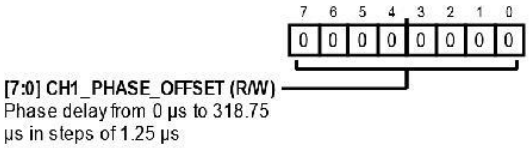
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH7_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x18 ; Reset: 0x80 ; Name: CH8_OFFSET



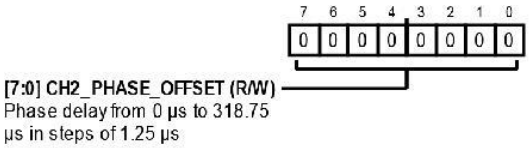
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH8_OFFSET	Offset register. Range is -128 LSB to +127 LSB. 0x00 = -128 LSB offset; 0x80 = no offset; 0xFF = +127 LSB offset.	0x80	R/W

Address: 0x19 ; Reset: 0x00 ; Name: CH1_PHASE



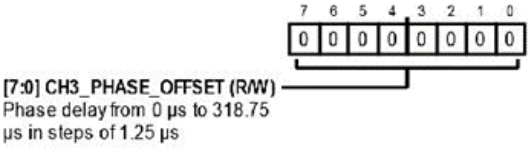
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH1_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1A ; Reset: 0x00 ; Name: CH2_PHASE



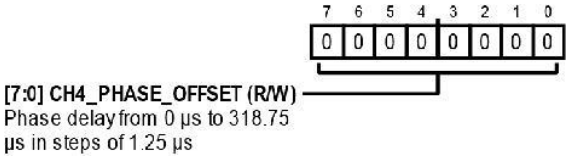
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH2_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1B ; Reset: 0x00 ; Name: CH3_PHASE



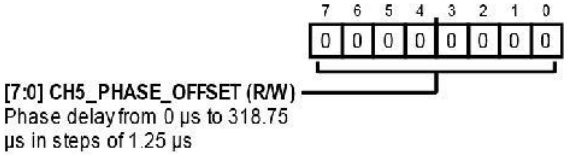
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH3_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1C ; Reset: 0x00 ; Name: CH4_PHASE



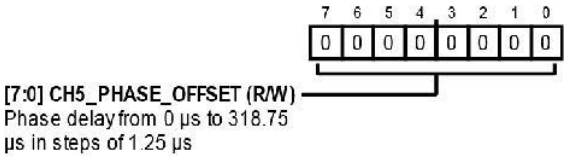
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH4_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1D ; Reset: 0x00 ; Name: CH5_PHASE



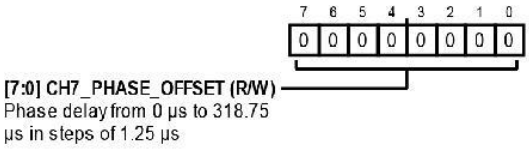
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH5_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1E ; Reset: 0x00 ; Name: CH6_PHASE



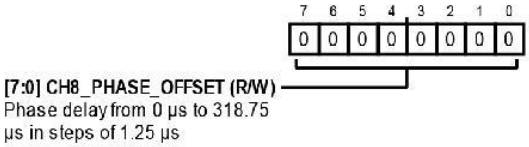
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH6_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1F ; Reset: 0x00 ; Name: CH7_PHASE



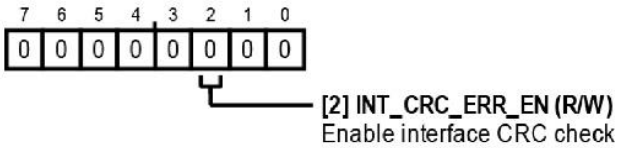
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH7_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x20 ; Reset: 0x00 ; Name: CH8_PHASE



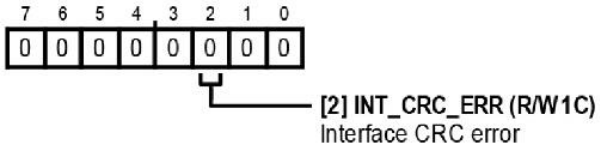
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CH8_PHASE_OFFSET	The phase delay ranges from 0 to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x21 ; Reset: 0x00 ; Name: DIGITAL_DIAG_ENABLE



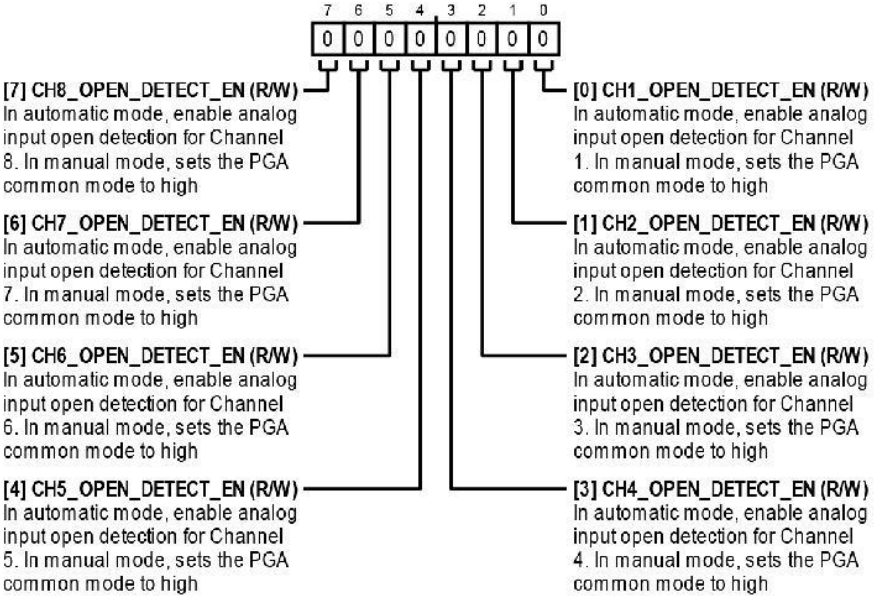
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:3]	RESERVED	RESERVED.	0x0	R/W
2	INT_CRC_ERR_EN	Enable interface CRC Error .	0x0	R/W
[1:0]	RESERVED	RESERVED.	0x0	R/W

Address: 0x22 ; Reset: 0x00 ; Name: DIGITAL_DIAG_ERR



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:3]	RESERVED	Reserved.	0x0	R/W
2	INT_CRC_ERR	Interface CRC Error.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R/W

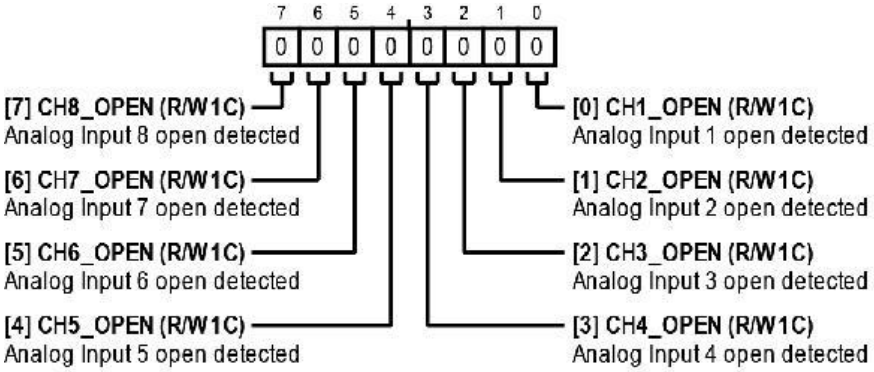
Address: 0x23 ; Reset: 0x00 ; Name: OPEN_DETECT_ENABLE



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
7	CH8_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for channel 8. In manual mode, set the PGA common mode high.	0x0	R/W
6	CH7_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for channel 7. In manual mode, set the PGA common mode high.	0x0	R/W
5	CH6_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for channel 6. In manual mode, set the PGA common mode high.	0x0	R/W
4	CH5_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for Channel 5. In manual mode, set the PGA common mode high.	0x0	R/W

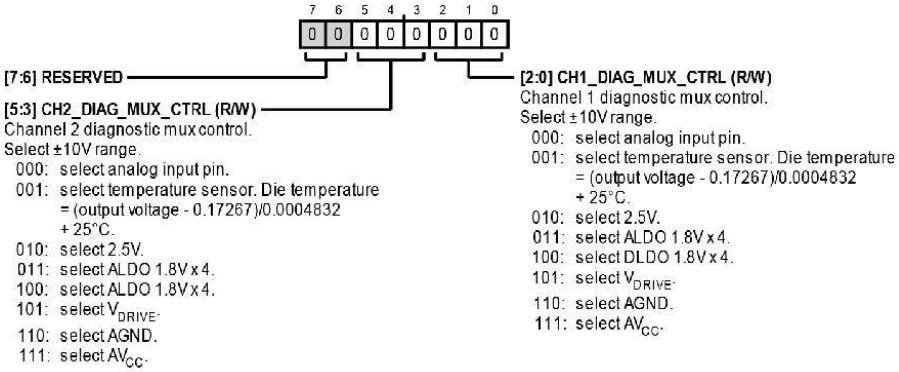
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
3	CH4_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for Channel 4. In manual mode, set the PGA common mode high.	0x0	R/W
2	CH3_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for channel 3. In manual mode, set the PGA common mode high.	0x0	R/W
1	CH2_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for channel 2. In manual mode, set the PGA common mode high.	0x0	R/W
0	CH1_OPEN_DETECT_EN	In automatic mode, enable analog input open wire detection for channel 1. In manual mode, set the PGA common mode high.	0x0	R/W

Address: 0x24 ; Reset: 0x00 ; Name: OPEN_DETECTED



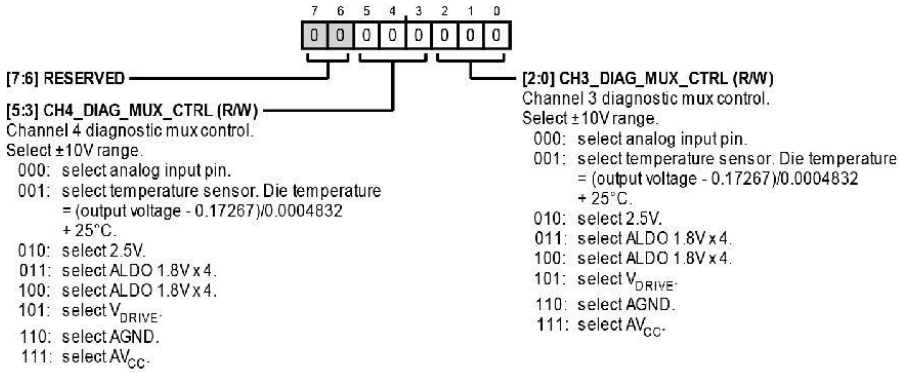
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
7	CH8_OPEN	An open circuit was detected on analog input 8.	0x0	R/W1C
6	CH7_OPEN	An open circuit was detected on analog input 7.	0x0	R/W1C
5	CH6_OPEN	An open circuit was detected on analog input 6.	0x0	R/W1C
4	CH5_OPEN	An open circuit was detected on analog input 5.	0x0	R/W1C
3	CH4_OPEN	An open circuit was detected on analog input 4.	0x0	R/W1C
2	CH3_OPEN	Analog Input 3 open circuit detected.	0x0	R/W1C
1	CH2_OPEN	Analog Input 2 open circuit detected.	0x0	R/W1C
0	CH1_OPEN	Analog Input 1 open circuit detected.	0x0	R/W1C

Address: 0x28 ; Reset: 0x00 ; Name: DIAGNOSTIC_MUX_CH1_2



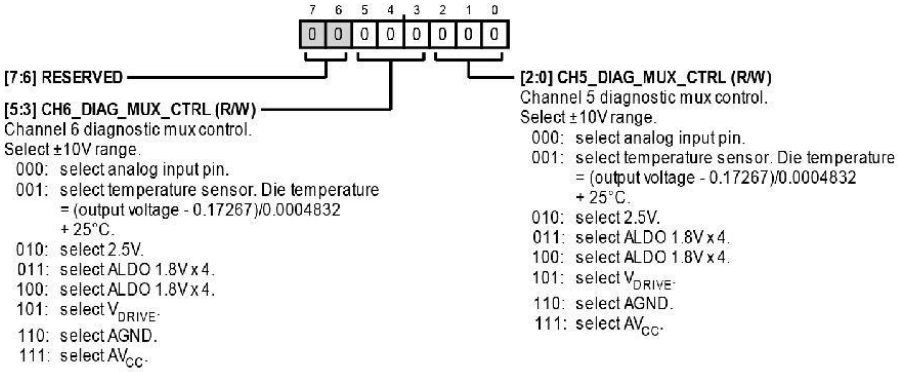
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:3]	CH2_DIAG_MUX_CTRL	Channel 2 diagnostic multiplexer control. Selects ±10 V range. 000: Select analog input pin. 001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C. 010: Select 2.5 V. 011: Select ALDO 1.8 V. 100: select ALDO 1.8 V. 101: Select V DRIVE . 110: Select AGND. 111: Select AV CC .	0x0	R/W
[2:0]	CH1_DIAG_MUX_CTRL	Channel 1 diagnostic multiplexer control. Selects ±10 V range. 000: Select analog input pin. 001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C. 010: Select 2.5 V. 011: Select ALDO 1.8 V. 100: Select DLDO 1.8 V. 101: Select V DRIVE . 110: Select AGND. 111: Select AV CC .	0x0	R/W

Address: 0x29 ; Reset: 0x00 ; Name: DIAGNOSTIC_MUX_CH3_4



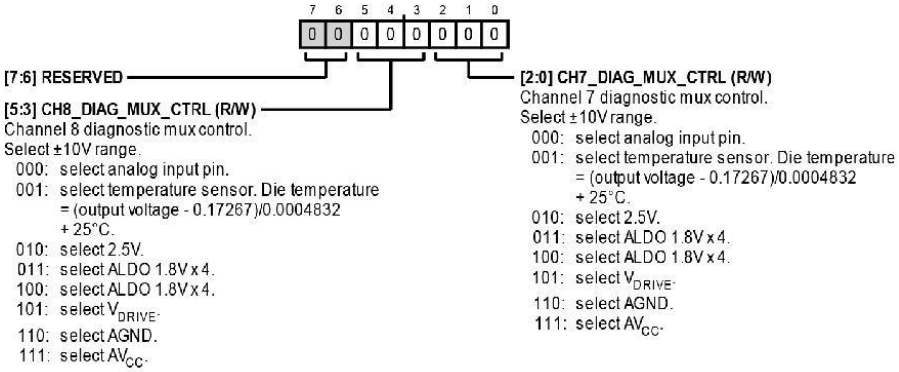
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:3]	CH4_DIAG_MUX_CTRL	Channel 4 diagnostic multiplexer control. Selects ±10 V range.	0x0	R/W
		000: Select analog input pin.		
		001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C.		
		010: Select 2.5 V.		
		011: Select ALDO 1.8 V.		
		100: select ALDO 1.8 V.		
		101: Select V_{DRIVE}.		
		110: Select AGND.		
		111: Select AV_{CC}.		
[2:0]	CH3_DIAG_MUX_CTRL	Channel 3 diagnostic multiplexer control. Selects ±10 V range.	0x0	R/W
		000: Select analog input pin.		
		001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C.		
		010: Select 2.5 V.		
		011: Select ALDO 1.8 V.		
		100: Select DLDO 1.8 V.		
		101: Select V_{DRIVE}.		
		110: Select AGND.		
		111: Select AV_{CC}.		

Address: 0x2A ; Reset: 0x00 ; Name: DIAGNOSTIC_MUX_CH5_6



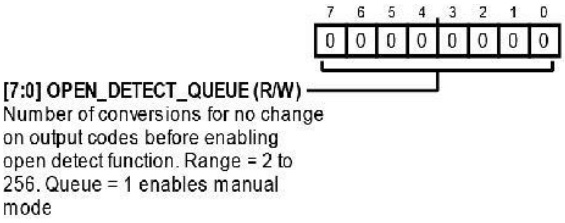
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:3]	CH6_DIAG_MUX_CTRL	Channel 6 diagnostic multiplexer control. Selects ±10 V range.	0x0	R/W
		000: Select analog input pin.		
		001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C.		
		010: Select 2.5 V.		
		011: Select ALDO 1.8 V.		
		100: select ALDO 1.8 V.		
		101: Select V_{DRIVE}.		
		110: Select AGND.		
		111: Select AV_{CC}.		
[2:0]	CH5_DIAG_MUX_CTRL	Channel 5 diagnostic multiplexer control. Selects ±10 V range.	0x0	R/W
		000: Select analog input pin.		
		001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C.		
		010: Select 2.5 V.		
		011: Select ALDO 1.8 V.		
		100: Select DLDO 1.8 V.		
		101: Select V_{DRIVE}.		
		110: Select AGND.		
		111: Select AV_{CC}.		

Address: 0x2B ; Reset: 0x00 ; Name: DIAGNOSTIC_MUX_CH7_8



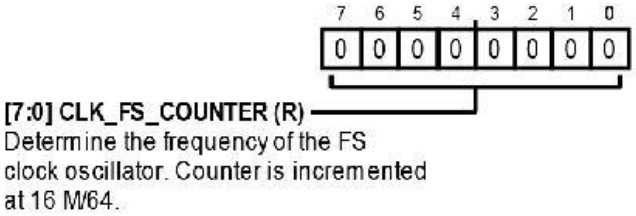
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:6]	RESERVED	reserve.	0x0	R
[5:3]	CH8_DIAG_MUX_CTRL	Channel 8 diagnostic multiplexer control. Selects ±10 V range.	0x0	R/W
		000: Select analog input pin.		
		001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C.		
		010: Select 2.5 V.		
		011: Select ALDO 1.8 V.		
		100: select ALDO 1.8 V.		
		101: Select V DRIVE .		
		110: Select AGND.		
		111: Select AV CC .		
[2:0]	CH7_DIAG_MUX_CTRL	Channel 7 diagnostic multiplexer control. Selects ±10 V range.	0x0	R/W
		000: Select analog input pin.		
		001: Select temperature sensor. Die temperature = (Output voltage − 0.17267)/0.0004832 + 25°C.		
		010: Select 2.5 V.		
		011: Select ALDO 1.8 V.		
		100: Select DLDO 1.8 V.		
		101: Select V DRIVE .		
		110: Select AGND.		
		111: Select AV CC .		

Address: 0x2C ; Reset: 0x00 ; Name: OPEN_DETECT_QUEUE



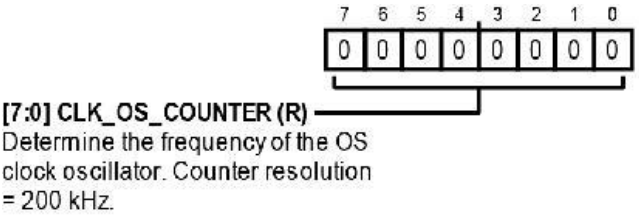
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	OPEN_DETECT_QUEUE	The number of transitions without output code change, after which the open circuit detection function is enabled. Range = 2 to 256. Queue = 1 enables manual mode.	0x0	R/W

Address: 0x2D ; Reset: 0x00 ; Name: FS_CLK_COUNTER



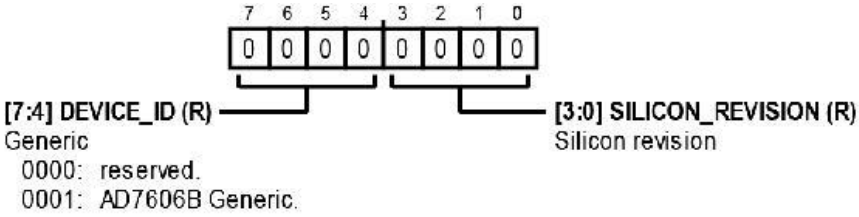
BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CLK_FS_COUNTER	Determines the frequency of the FS clock oscillator. The counter increments by 16 M/64.	0x0	R

Address: 0x2E ; Reset: 0x00 ; Name: OS_CLK_COUNTER



BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:0]	CLK_OS_COUNTER	Determines the frequency of the OS clock oscillator. Counter resolution = 200 kHz.	0x0	R

Address: 0x2F ; Reset: 0x14 ; Name: ID

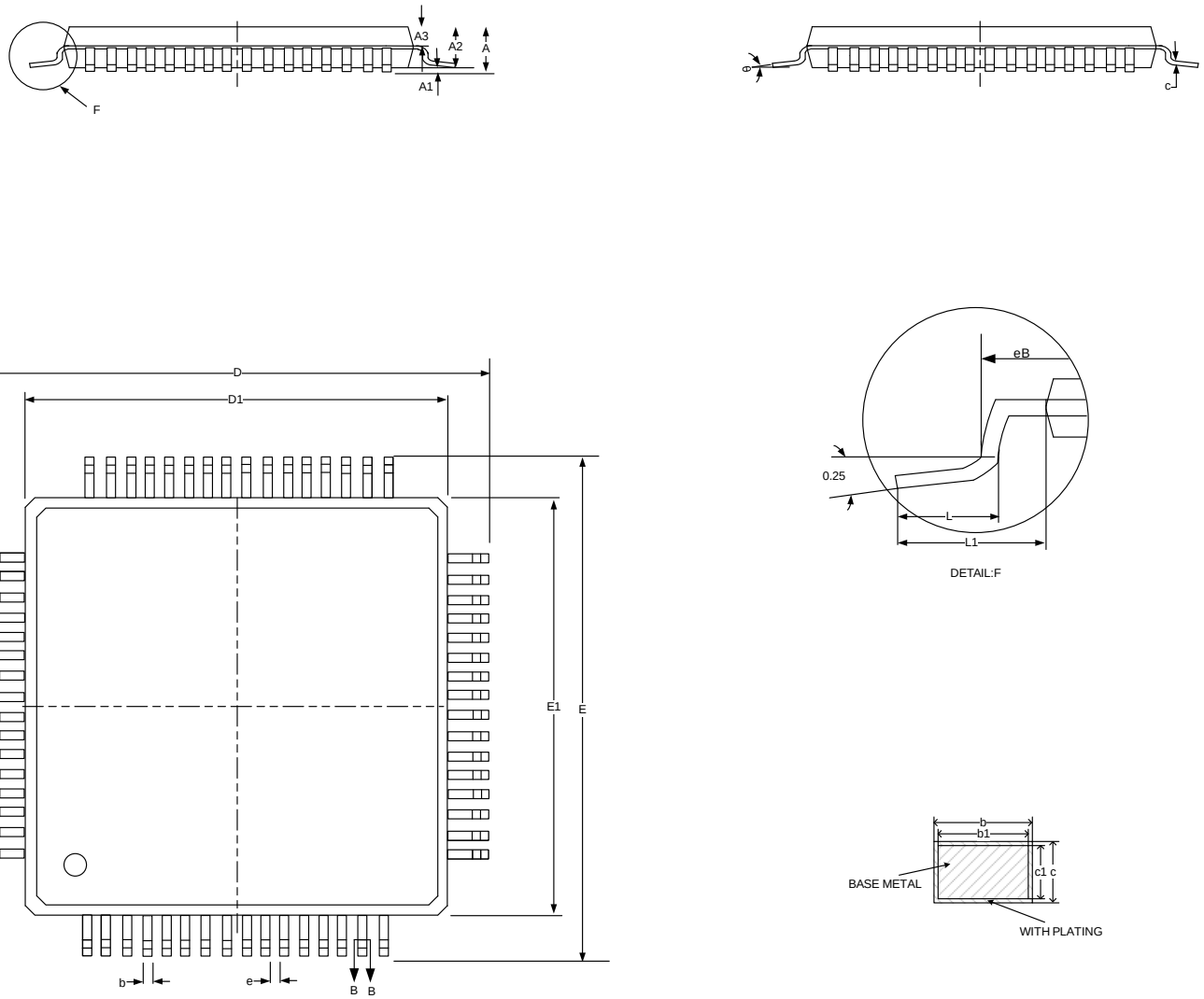


BIT	BIT NAME	DESCRIBE	RESET	ACCESS TYPE
[7:4]	DEVICE_ID	General. 0000: Reserved. 0001: GD30AD3380 General	0x1	R
[3:0]	SILICON_REVISION	Chip version.	0x0	R

15 Packaging information

15.1 Outline Dimensions

LQFP64



NOTES:

1. All dimensions are in millimeters (mm).
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to Table 22. *LQFP64 dimensions (mm)*.

Table 22. LQFP64 dimensions (mm)

SYMBOL	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18		0.26
b1	0.17	0.20	0.23
c	0.13		0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.5 BSC		
eB	11.05		11.25
L	0.45		0.75
L1	1.00REF		
θ	0°		7°

16 Ordering Information

Ordering Code	Package Type	ECO Plan	Packaging Type	MOQ	OP Temp (°C)
GD30AD3380RWTR-I05	LQFP64	Green	Tape & Reel	1500	−40°C to +125°C
GD30AD3380RWTR-I10	LQFP64	Green	Tape & Reel	1500	−40°C to +125°C

17 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024
1.1	1. Modify the content for GD30AD3380-I10 and GD30AD3380-I05 separately, providing distinct explanations for each. 2. Update the readability of all images.	2024

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the "Product"), is owned by the Company according to the laws of the People's Republic of China and other applicable laws. if any) are the property of their respective owners and referred to for identification purposes only.

The Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. Unless otherwise expressly specified in the datasheet of the Product, the Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.