16-Bit、8-Channel、500 KSPS、SAR ADC

1 Features

- 16-bit resolution, no missing codes
- 8-channel multiplexer with selectable inputs
  - Single-ended
  - Differential (relative to GND)
  - Pseudo differential
- Throughput
  - 250 KSPS (GD30AD3382-I02)
  - 500 KSPS (GD30AD3382-I05)
- INL: ±0.5 LSB typical, ±1.5 LSB maximum (±23 ppm or FSR)
- Dynamic range: 93.3 dB
- SINAD: 91.5 dB@20 KHz
- THD: 97 dB@20 KHz
- Analog input range: 0V - VREF, VREF can be to VDD
- Various reference voltage types
  - Internal 4.096 V
  - External buffer (up to 4.096 V)
  - External (highest VDD)
- Internal temperature sensor
- Channel sequencer, optional single-ended filter, pipeline without delay Busy indicator, SAR structure
- Single power supply 5 V
  - 1.8 V to 5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, DSP
- Power consumption
  - 26 mW @ 500 kSPS
  - 5.2 μW@ 100 SPS
- Standby current: 50 nA
- 20-lead 4 mm × 4 mm QFN package

2 Application

- Battery-powered devices Medical instruments: ECG/EKG
- Mobile communications: GPS
- Power Line Monitoring Data Collection for Personal Digital Assistants
- Seismic Data Acquisition System Instrumentation
- Process Control

3 Description

The GD30AD3382 is an 8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) powered by a single power supply, VDD. The GD30AD3382 contains all the components for a multi-channel, low-power data acquisition system, including a true 16-bit SAR ADC with no missing codes; an 8-channel low-crosstalk multiplexer for configuring inputs as single-ended (referenced or not referenced to GND), differential, or bipolar inputs; an internal 4.096 V low-drift reference source as well as output buffers and temperature sensors; an optional single-pole filter; and a sequencer for continuous scanning in channel order.

GD30AD3382 uses a simple serial port interface (SPI) to write configuration registers and receive conversion results. The SPI interface uses a separate power supply VIO, the same as the host port power supply. Power consumption varies with throughput.

The GD30AD3382 is packaged in a 20-pin QFN and operates over the −40 °C to +125 °C temperature range.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AD3382	QFN20	4.00mm x 4.00mm

1. For packaging details, see *Packaging Information* section .

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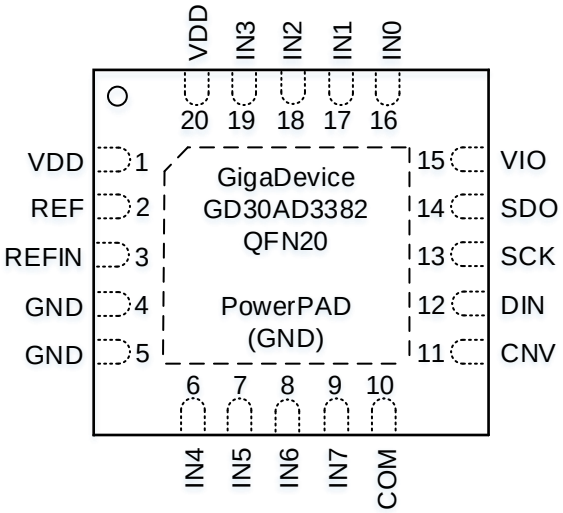
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PINS		PIN TYPE[1]	FUNCTION
NAME	NUM		
VDD	1, 20	P	Supply Voltage. 4.5 V to 5.5 V nominal, 10 µF and 100 nF decoupling capacitors in parallel are required.
REF	2	AI / O	For reference source input/output, see *Voltage Reference Output/Input* section for details. When the internal reference source is enabled, the REF pin outputs a 4.096 V internal reference source voltage. When the internal reference source is not enabled, the reference source output buffer is enabled, and the REF pin serves as the output of the buffer, outputting the voltage on the REFIN pin (maximum VDD-0.5V). This configuration is very useful in low-cost, low-power scenarios. If you need to improve the temperature drift characteristics, the REF pin can be directly connected to a precise reference source (0.5V to VDD). In any mode, the REF pin needs to be connected in parallel with a 10 bF decoupling capacitor and as close to the REF pin as possible. See *Reference Source Decoupling Capacitor* section for details .
REFIN	3	AI / O	Internal reference source output/reference source buffer input. When the internal reference source is enabled, the REFIN pin outputs the reference source voltage without passing through the reference source output buffer, and a 0.1 µF decoupling capacitor is required in parallel.
GND	4, 5	P	Ground.
IN4 to IN7	6 to 9	AI	Mode input channels 4 to 7.

PINS		PIN TYPE[1]	FUNCTION
NAME	NUM		
COM	10	AI	Common-mode voltage channel inputs. All input channels IN[7:0] can be referenced to a common-mode voltage of 0 V or VREF/2 V.
CNV	11	DI	Input for conversion. On a rising edge, CNV starts a conversion. During a conversion, if CNV is held high, the busy indication is enabled.
DIN	12	DI	Data Input. Serves as a 14-bit configuration register value input pin. The configuration register can be written during and after conversion.
SCK	13	DI	Serial Data Clock Input.
SDO	14	DO	Serial data output. The conversion result is output on this pin and is synchronized with SCK. The conversion result of single-ended mode is binary code, and the conversion result of differential mode is two's complement code.
VIO	15	P	Input/output interface digital power supply voltage. Usually consistent with the host structure voltage (1.8V, 2.5V, 3V or 5V).
IN0 to IN3	16 to 19	AI	Analog input channels 0 to 3.
EPAD	21	P	There is no connection internally. To increase the reliability of the solder joint, it is recommended to butt the pad to the GND plane.

1. AI = Analog Input, AI /O = Analog Input/Output, DI = Digital Input, DO = Digital Output, P = Power.

5 Parameter Information

5.1 Absolute Maximum Ratings

PARAMETER	RATING
INx[1] , COM[1]	GND − 0.3 V to VDD+0.3 V or VDD±130 mA
REF, REFIN	GND − 0.3 V to VDD + 0.3 V
VDD, VIO to GND	−0.3 V to +7 V
From VDD to VIO	±7 V
DIN, CNV, SCK to GND	−0.3 V to VIO+0.3 V
SDO to GND	−0.3 V to VIO+0.3 V
Storage temperature range	−65 °C to +150 °C
Junction temperature	150 °C
Human Body Model (HBM)	1500 V
Machine Discharge Mode (MM)	200 V
Charge Field Model (CDM)	1500 V

1. See *Input Configuration* section.

5.2 Thermal Resistance

PACKAGE	θ_{JA}[1]	θ_{JC}[1]	UNIT
QFN20	46.8	0.7	°C/W

1. Test conditions Thermal impedance simulation values are based on the 2S2P JEDEC PCB.

5.3 Electrical Specifications

VDD = 4.5 V to 5.5 V, VREF = 4.096 V to VDD, VIO = 1.8 V to VDD, all specifications over −40 °C to +105 °C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		16			Bits
Analog Input					
Voltage range	Single-ended mode	0		+VREF	V
	Differential Mode	−VREF/2		+VREF/2	V
Absolute input voltage	Positive input, single-ended and differential modes	−0.1		VREF + 0.1	V
	Negative input or COM input, single-ended mode	−0.1		+0.1	V
	Negative input or COM input, differential mode	VREF/2 − 0.1	VREF/2	VREF/2 + 0.1	V
Analog Input CMRR	f_{IN} = 250 kHz		68		dB
Input leakage current 25°C	Sampling stage		1		nA

Electrical Specifications (Continued)

VDD = 4.5 V to 5.5 V, VREF = 4.096 V to VDD, VIO = 1.8 V to VDD, all specifications over -40 °C to +105 °C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Throughput					
Full Bandwidth[2]		0		500	kSPS
1/4 bandwidth[2]		0		125	kSPS
Accuracy					
No missing codes		16			Bits
Integral linearity error		−2	±0.5	+1	LSB[3]
Differential Nonlinearity		−0.5	±0.25	+0.5	LSB
Gain Error		−10	±1	+10	LSB
Gain Error Mismatch		−2	±1	+2	LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Offset Error	All modes	−8	±1	+8	LSB
Offset Error Mismatch		−2	±1	+2	LSB
Offset Error Temperature Drift			±0.3		ppm/°C
Power supply sensitivity	VDD = 5 V ± 5 %		±1.5		LSB
AC Characteristics					
Dynamic Range			93		dB[4]
Signal-to-Noise Ratio	f_{IN} = 1 kHz, VREF = 5 V	91	92		dB
	f_{IN} = 1 kHz, VREF = 4.096 V internal REF	89	91		dB
Signal-to-Noise-Distortion Ratio					
Signal-to-Noise-Distortion Ratio	f_{IN} = 1 kHz, VREF = 5 V	90	91.5		dB
	f_{IN} = 1 kHz, VREF = 4.096 V internal REF	88	90.5		dB
Total Harmonic Distortion	f_{IN} = 1 kHz		−110		dB
Spurious Free Dynamic Range	f_{IN} = 1 kHz		110		dB
Channel Crosstalk	f_{IN} =100 kHz Adjacent channel		−120		dB
Internal reference source					
REF output voltage	at 25 °C	4.090	4.096	4.102	V
REFIN output voltage	at 25 °C		2.3		V
REF output current			±300		µA
Temperature drift			±5		ppm/°C

Electrical Specifications (Continued)

VDD = 4.5 V to 5.5 V, VREF = 4.096 V to VDD, VIO = 1.8 V to VDD, all specifications over -40 °C to +105 °C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Long-term drift	1000 hours		50		ppm
Power-on setup time	CREF = 10 µF		5		ms
External Reference Source					
Voltage range	REF Input	2.4		VDD + 0.3	V
	REFIN input (buffered)	2.4		VDD − 0.2	V
Input Current	500 kSPS, REF = 5V		100		µA
Temperature Sensor					
Output voltage[5]	at 25°C		300		mV
Temperature sensitivity			1		mV/°C
Digital Input					
V_{IL}		−0.3		+0.3 × VIO	V
V_I		0.7×VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
Digital Output					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V	I_{SOURCE} = − 500 µA	VIO − 0.3			V
power supply					
VDD	Performance Guarantee	4.5		5.5	V
VIO	Performance Guarantee	1.8		VDD + 0.3	V
Standby current [9,10]	at 25°C, VDD and VIO = 5 V		50		nA
Power consumption	VDD = 5 V, 100 kSPS		5.2		µW
	VDD = 5 V, 500 kSPS		14.5	18	mW
	VDD = 5 V, 500 kSPS, internal reference		16.5	21	mW
Temperature range					
Performance Guarantee	T_{MIN} to T_{MAX}	−40		+125	°C

1. See the Analog Input section.
2. The bandwidth is set by the configuration register.
3. LSB stands for Least Significant Bit. When the input voltage is 5V, 1 LSB = 76.3µV.
4. Unless otherwise specified, all specifications expressed in decibels are referenced to full-scale input FSR and are tested with an input signal 0.5 dB below full scale.
5. This is the output of the internal reference source.
6. The internal output voltage is fed to specific multiplexer inputs.
7. Single-ended mode: serial 16-bit binary code. Differential mode: serial 16-bit two's complement code.

8. The conversion results are available immediately after the conversion is completed.
9. All digital inputs are forced to VIO or GND as required.
10. In the sampling phase.

5.4 Timing Specifications

5.4.1 General Timing Specifications

VDD = 4.5 V to 5.5 V, VREF = 4.096 V to VDD, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER[1]	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion Time: CNV Rising Edge to Data Available			1.55	μs
t_{ACQ}	Data collection time	450			ns
t_{CYC}	Time between transitions[2]	2			μs
t_{CNVH}	CNV pulse width	10			ns
t_{DATA}	Data write/read during conversion			1.2	μs
t_{SCK}	SCK cycle	t_{DSDO} + 2			ns
t_{SCKL}	SCK low time	11			ns
t_{SCKH}	SCK High Time	11			ns
t_{HSDO}	SCK falling edge to data valid	4			ns
t_{DSDO}	SCK falling edge to data valid delay				
	VIO is above 4.5 V			16	ns
	VIO is above 3 V			17	ns
	VIO is above 2.7 V			18	ns
	VIO is above 2.3 V			21	ns
	VIO is above 1.8 V			28	ns
t_{EN}	CNV Low to SDO D15 MSB Valid				
	VIO is above 4.5 V			15	ns
	VIO is above 3 V			17	ns
	VIO is above 2.7 V			18	ns
	VIO is above 2.3 V			22	ns
	VIO is above 1.8 V			25	ns
t_{DIS}	CNV high or last SCK falling edge to SDO high impedance			32	ns
t_{CLSCK}	CNV Low to SCK Rising Edge	10			ns
t_{QUIET}	Delay from the last SCK falling edge to the CNV rising edge	40			ns
t_{SDIN}	DIN valid setup time from SCK rising edge	5			ns
t_{HDIN}	DIN valid hold time from SCK rising edge	5			ns

1. The loading conditions are shown in Figure 1 and Figure 2.

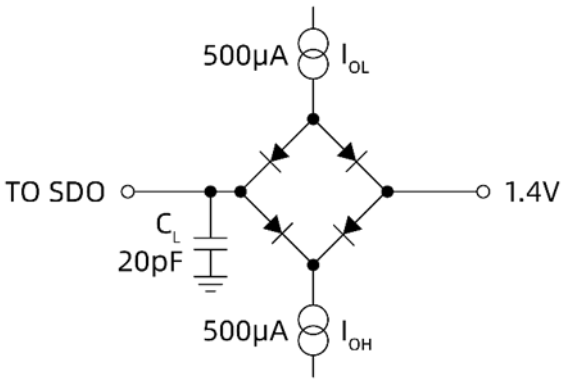


Figure 1. Digital Interface Timing

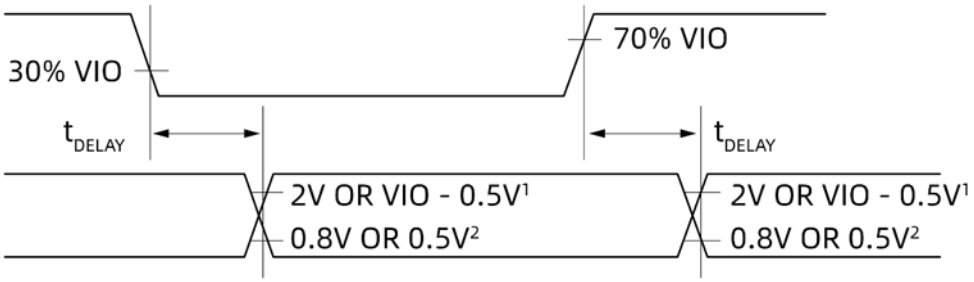


Figure 2. Voltage Levels for Timing Rev.G

1. 2 V when VIO is above 2.5 V, 0.5 V when VIO is below 2.5 V.
2. 0.8 V when VIO is above 2.5 V, 0.5 V when VIO is below 2.5 V.

5.5 Typical Performance Characteristics

V_{REF} = 5 V, V_{DD} = 5 V, VIO = V_{DD}, unless otherwise noted.

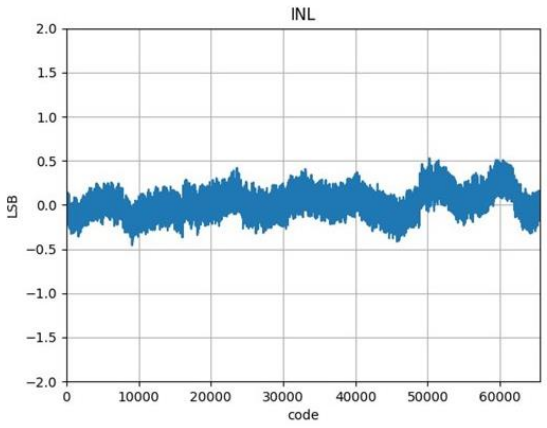


Figure 3. INL vs. Code

(VDD=5V, VREF= internal 4.096V)

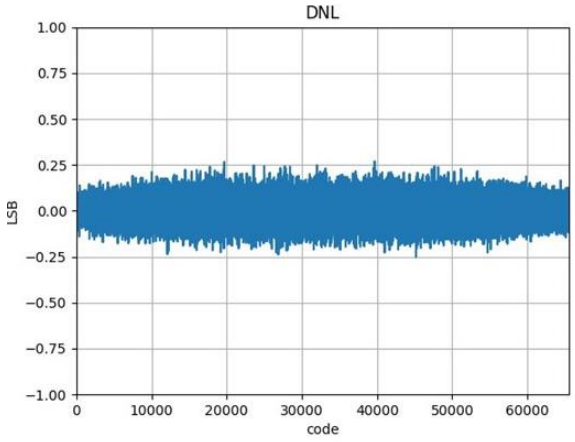


Figure 4. DNL vs. Code

(VDD=5V, VREF= internal 4.096V)

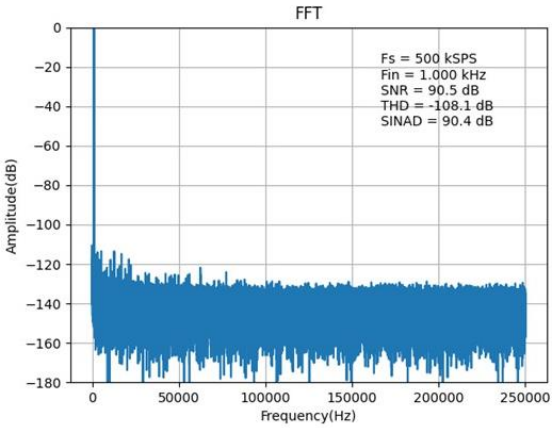


Figure 5. FFT (VDD=5V, VREF= internal 4.096V)

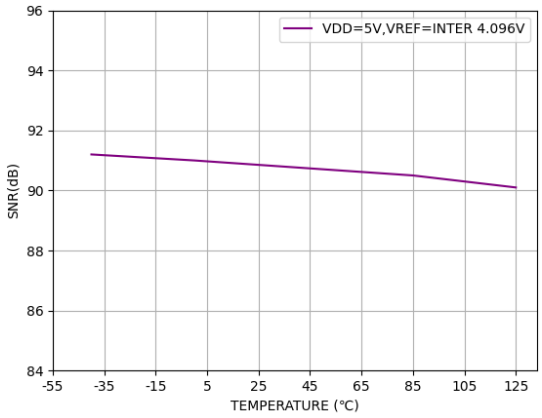


Figure 6. SNR vs. Temperature

Typical Performance Characteristics (Continued)

V_{REF} = 5 V, V_{DD} = 5 V, VIO = V_{DD}, unless otherwise noted.

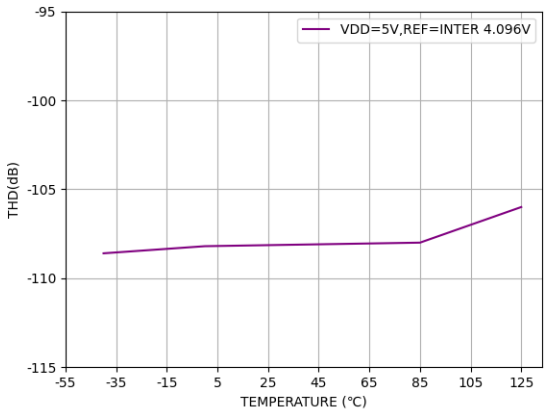


Figure 7. THD vs. Temperature

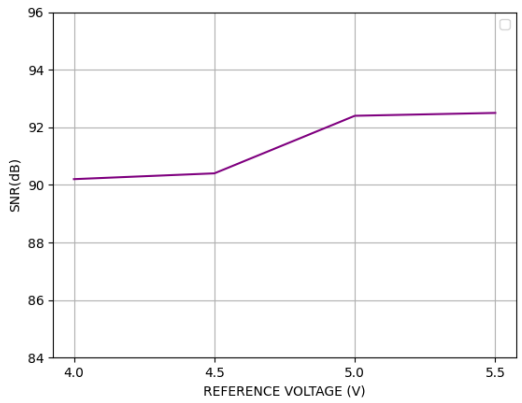


Figure 8. SNR vs. Reference Voltage

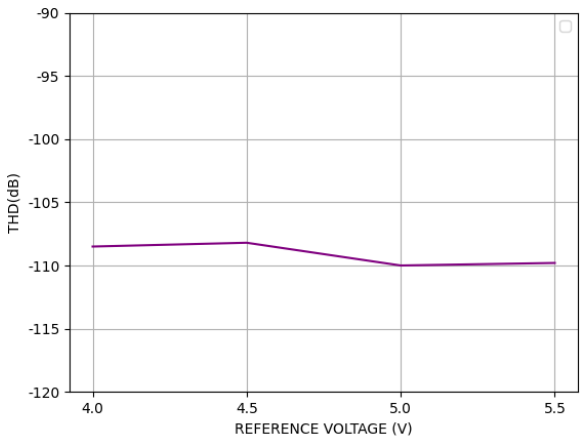


Figure 9. THD vs. Reference Voltage

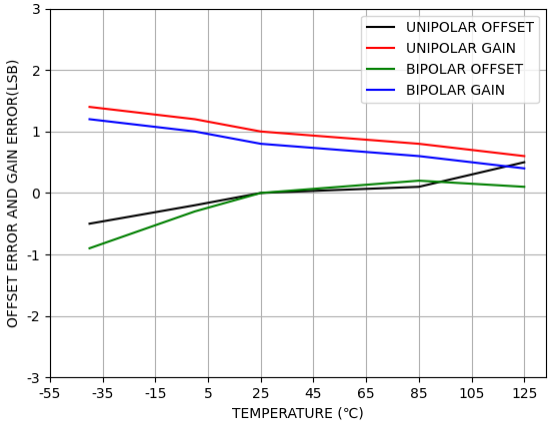


Figure 10. Offset and Gain Errors vs. Temperature

Typical Performance Characteristics (Continued)

V_{REF} = 5 V, V_{DD} = 5 V, VIO = V_{DD}, unless otherwise noted.

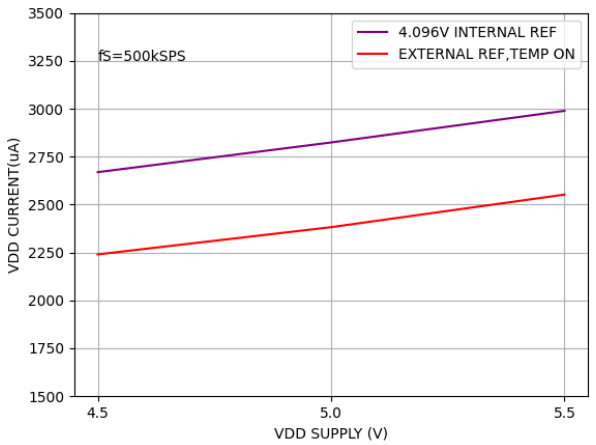


Figure 11. Operating Currents vs. VDD Supply

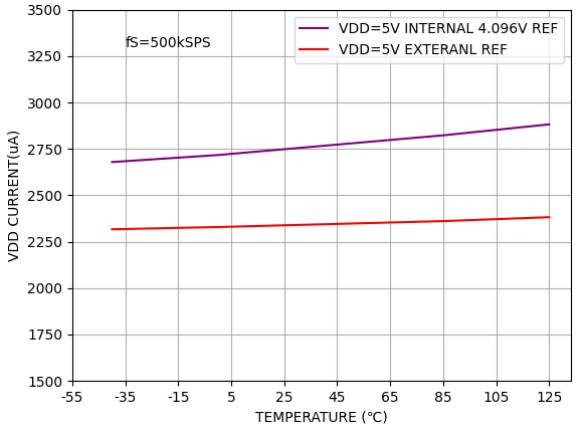


Figure 12. Operating Currents vs. Temperature

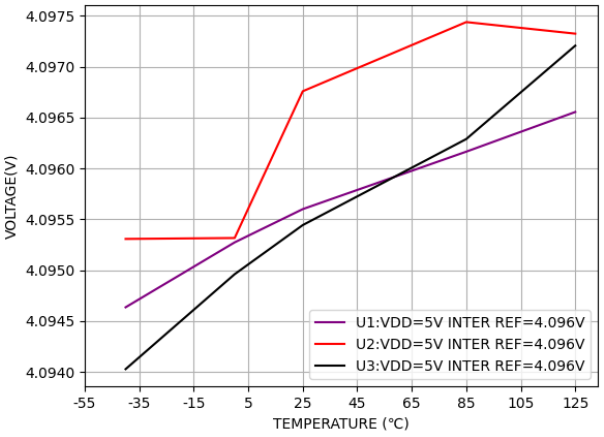


Figure 13. Internal Reference Output Voltage vs. Temperatur

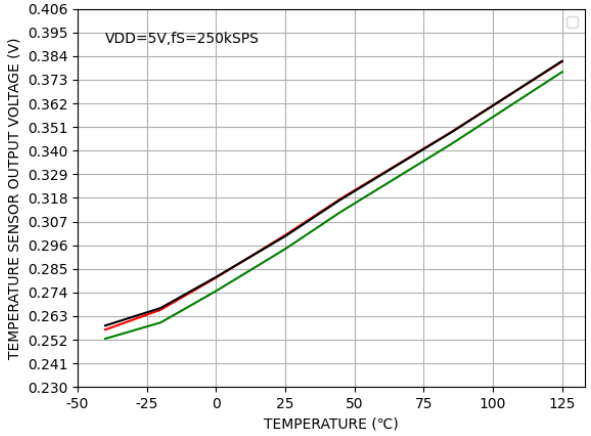


Figure 14. Temperature Sensor Output Voltage vs. Temperature

6 Functional Description

6.1 Block Diagram

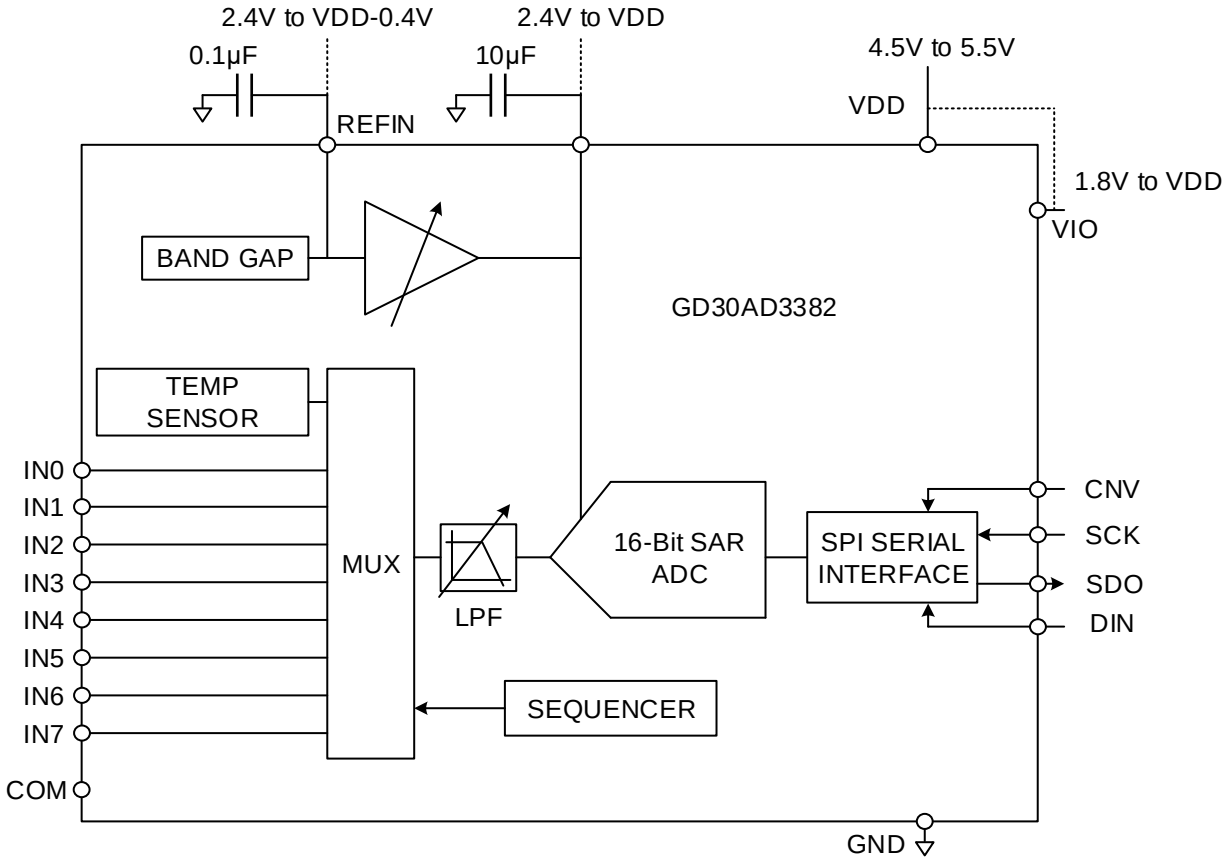


Figure 15. GD30AD3382 Functional Block Diagram

6.2 Operation

6.2.1 Overview

The GD30AD3382 is an 8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC). It is capable of converting 500,000 samples per second (500 kSPS) and can be powered down between conversions. For example, when using an external reference source at a conversion rate of 1 kSPS, it typically consumes 52 μW, making it ideal for battery-powered applications.

The GD30AD3382 contains all the components required for a multi-channel, low-power data acquisition system, including:

- 16-bit SAR ADC with no missing codes
- 8-Channel Low Crosstalk Multiplexer
- Internal low drift reference and output buffer
- Temperature Sensor
- Optional single stage filter
- Channel Sequencer

These components configure the 14-bit registers via SPI. The conversion results can also be read via SPI after or during the conversion by the readback configuration option.

6.2.2 Transfer Function

The input is configured in single-ended mode (single-ended, COM referenced to GND, or differential, INx-relative to GND), and the data output is binary.

If the input is configured in differential mode (COM = V_{REF} / 2 or differential INx- = V_{REF} / 2), the data output is two's complement.

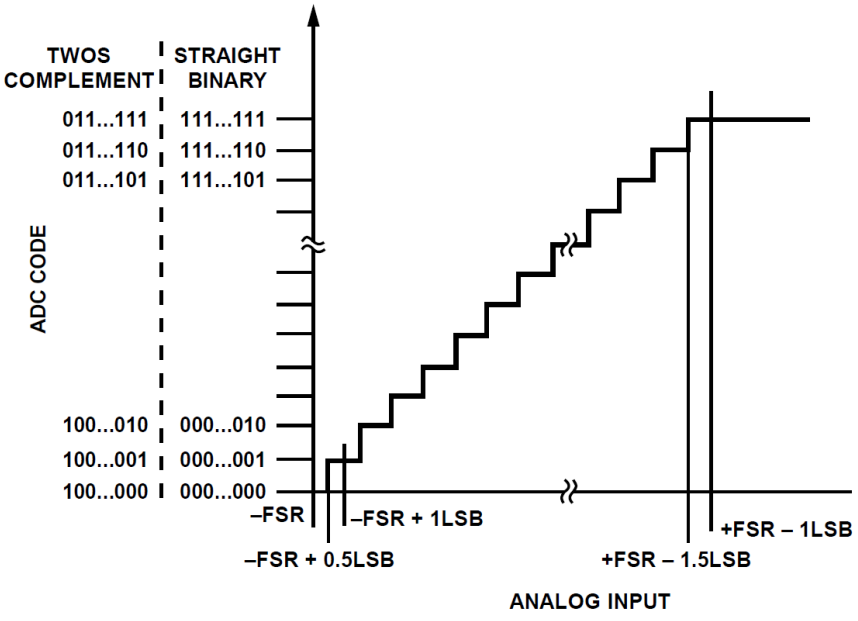


Figure 16. ADC Ideal Transfer Function

Table 1. Output Codes and Ideal Input Voltages

Description	Single-ended analog input[1] VRFE = 4.096V	Digital output code (Straight Binary Hex)	Differential analog input[2] VREF = 4.096V	Digital output code (Twos Complement Hex)
FSR − 1LSB	4.095938 V	0xFFFF[3]	2.047938 V	0x7FFF[3]
Midscale + 1LSB	2.048063 V	0x8001	62.5μV	0x0001
Midscale	2.048 V	0x8000	0 v	0x0000
Midscale − 1LSB	2.047938 V	0x7FFF	− 62.5μV	0xFFFF[4]
− FSR + 1LSB	62.5μV	0x0001	− 2.047938 V	0x8001
− FSR	0 v	0x0000 [3]	− 2.048 V	0x8000

1. COM or INx− = 0v or all INx referenced to GND.
2. Use COM or INx− = VREF/2.
3. This is also a COM higher than the analog input ((INx+)-(INx−), or above V, (REF −VGND).
4. This is also below the analog input ((INx+) - (INx−) or COM, and below GND.

6.3 Typical Application Diagram of Multiple Power Supplies

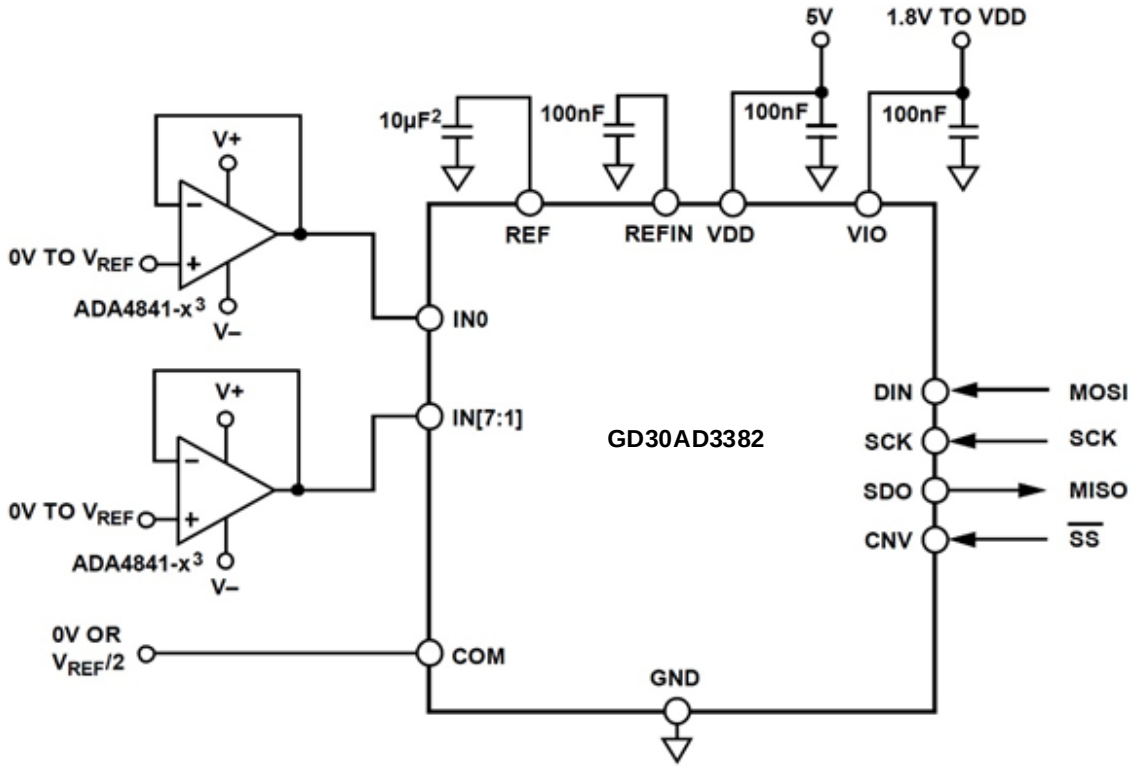


Figure 17. Typical Application Diagram of Multiple Power Supplies

1. Internal reference source mode, see *Voltage Reference Output/Input* Selection for details.
2. Cref is typically a 10 μF ceramic capacitor (X5R).
3. See the *Digital Interface* section for configuration and reading conversion data.

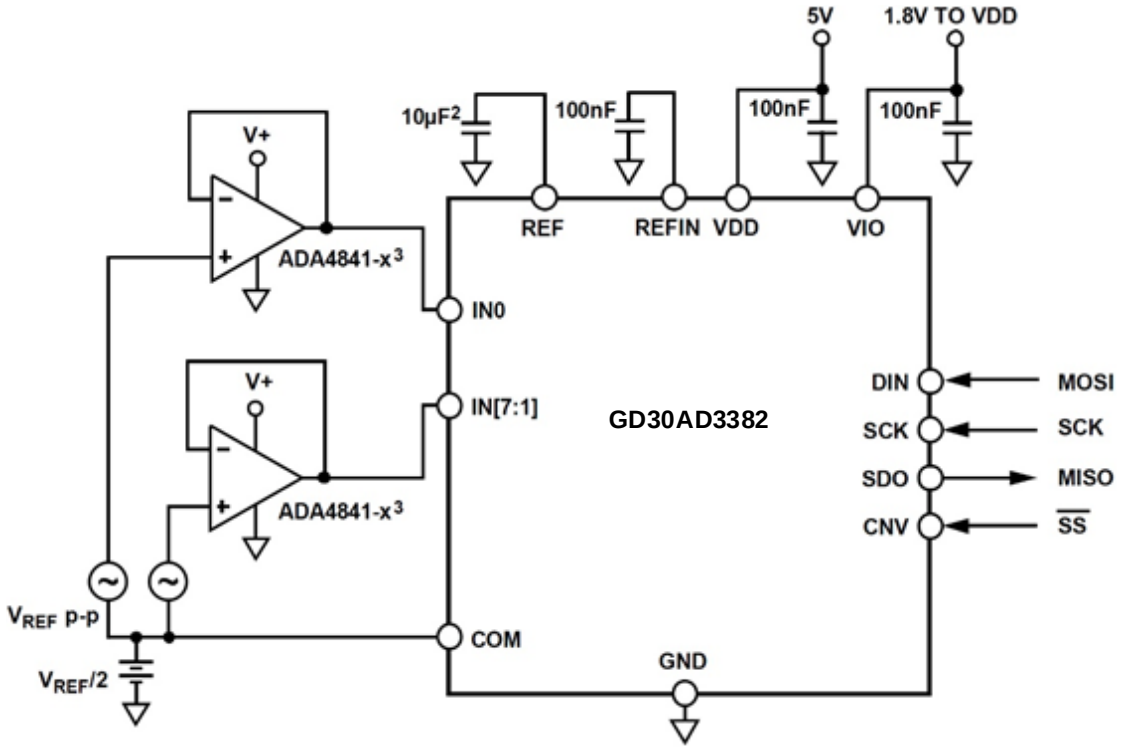


Figure 18. Diagram Using Differential Input

1. Internal reference source mode, see *Voltage Reference Output/Input* selection for details
2. Cref is typically a 10 µF ceramic capacitor (X5R).
3. See the *Digital Interface* section for configuration and reading conversion data.

6.3.1 Single-ended or Differential

Figure 17 shows an example of a recommended connection diagram for the GD30AD3382 when multiple power supplies are available.

6.3.2 Single-ended Single Supply

Figure 18 shows an example of a system with single-ended inputs that enables the internal reference source to operate from a single supply (different VIO supply optional). This circuit is also useful when the amplifier/signal conditioning circuit is remotely located and some common mode is present. Note that for any input configuration, the INx inputs are single-ended and are always referenced to GND (no negative voltages even in the differential range).

For this circuit, a rail-to-rail input/output amplifier can be used. However, care must be taken and consideration must be given to the offset voltage and input common-mode range (1 LSB = 62.5 µV with VREF = 4.096 V). When a differential input configuration is used, the conversion result is in two's complement format.

6.3.3 Input Configuration

Figure 19 shows the different ways to configure the analog inputs using the configuration register (CFG[12:10]). Refer to *Configuration Register CFG* section for more information.

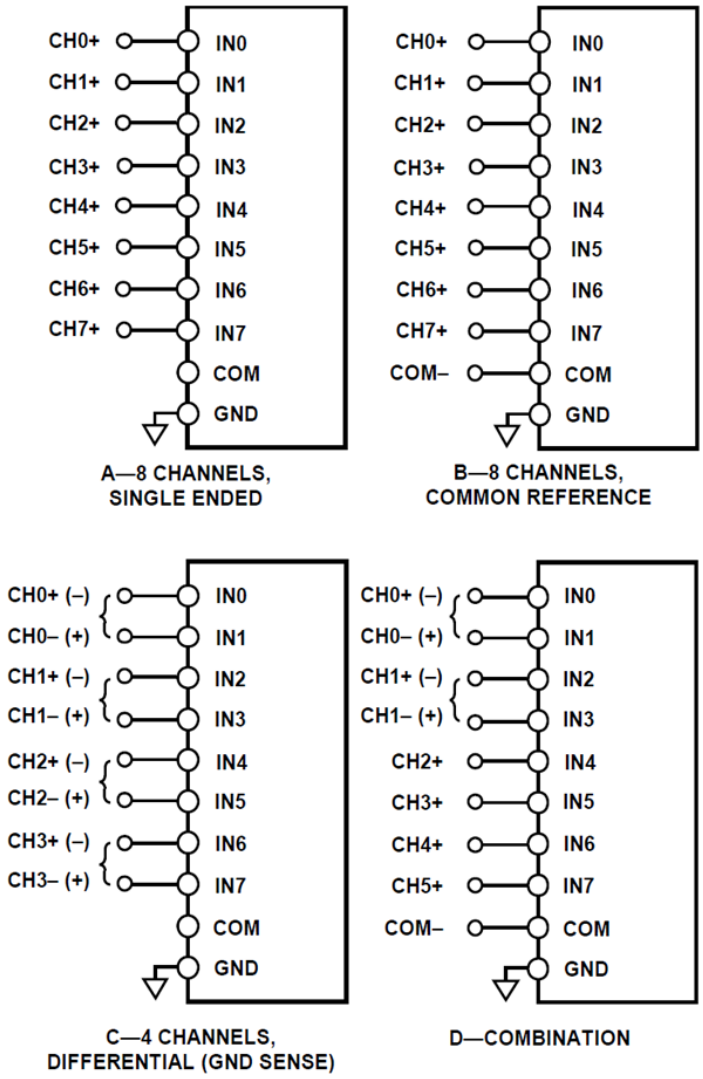


Figure 19. Multiplexed Analog Input Configuration

The GD30AD3382 analog input can be configured in single-ended or pseudo-differential mode, which means that the positive input pin of the GD30AD3382 can accept a signal between 0 V and VREF, and its negative input (or COM) pin must always be referenced to ground or a fixed DC voltage VREF/2, as shown below:

- Figure 19: Single-ended with respect to system ground ; CFG[12:10] = 111.
- Figure 19: Differential inputs with common reference point ; COM = VREF/2 ; CFG[12:10] = 010. Differential with respect to COM, COM connected to GND; CFG[12:10] = 110.
- Figure 19: Differential input INx- relative to VREF/2 ; CFG[12:10] = 00X. Differential input INx- referenced to GND; CFG[12:10] = 10X. In this configuration, INx+ is configured by CFG[9:7]. For example, for IN0 = IN1+, IN1 = IN1−, CFG[9:7] = 000 ; for IN1 = IN1+ and IN0 = IN1− , CFG[9:7] = 001.
- Figure 19: The input configuration is any combination of the above (indicating that the GD30AD3382 can be dynamically configured).

6.3.4 Sequencer

The GD30AD3382 includes a channel sequencer that can be used to scan channels in the manner of IN0 to IN[7:0]. After determining the last channel of the sequence, the channels are scanned one by one or in pairs, including or excluding the temperature sensor.

The sequencer starts at IN0 and ends at IN[7:0] set by CFG[9:7]. For paired channels, the channel pairing is determined by the last channel set in CFG[9:7]. Note that the channel pair is always paired in the manner of IN(even) = INx+ and IN(odd) = INx−, regardless of the contents of CFG[7].

To enable the sequencer, write to CFG[2:1] to initialize it. After CFG[13:0] is updated, DIN must be low when reading data (at least bit 13), otherwise the CFG register will start updating again.

When operating in sequence mode, the CFG register contents can be changed by writing 2'b01 to CFG[2:1]. However, if CFG[11] (paired or single channel) or CFG[9:7] (last channel in sequence) is changed, the sequence is reinitialized and IN0 (or IN1) is converted after the CFG is updated.

6.3.5 Example

Bit[13], Bits[6:3], and Bit 0 are configured as input and sequencer mode.

As a first example, reference COM = GND and scan all IN[7:0] and the temperature sensor.

Table 2.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC			INx			BW	REF			SEQ		RB
	1	1	0	1	1	1					1	0	

As a second example, scan three paired channels, without a temperature sensor, and referenced to VREF/2.

Table 3.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC			INx			BW	REF			SEQ		RB
	0	0	X [1]	1	0	X [1]					1	1	

1. X means don't care.

6.4 Voltage Reference Output/Input

The GD30AD3382 allows the selection of an extremely low temperature drift internal voltage reference source, an external reference source, or an external buffered reference source.

The GD30AD3382's internal reference source provides excellent performance and can be used in almost all applications.

6.4.1 Internal Reference Source/Temperature Sensor

The internal reference value can be set to 4.096 V output, see Table 4. When the internal reference is enabled, the bandgap reference voltage is output on the REFIN pin and requires an external parallel 0.1 μF capacitor.

Enabling the internal reference also enables the internal temperature sensor, which measures the internal temperature of the GD30AD3382 and is therefore useful for performing system calibration. For applications that require the use of a temperature sensor, the internal reference source must be enabled (the internal reference source buffer can be disabled in this case). Note that when the temperature sensor is used, the output is in single-ended input conversion mode and the conversion result is a binary code because the reference voltage is the GD30AD3382 GND pin. The voltage of the GD30AD3382 temperature sensor can be regarded as a normal analog input; therefore, the conversion result code representing it is calculated as the temperature sensor code = Temperature sensor voltage x (reference voltage) / (2^16-1). Its temperature sensor output voltage is typically 283

mV at 25 °C. The internal reference source temperature can be compensated to within 10 mV. The internal reference source voltage can be trimmed to provide a typical temperature drift characteristic of ±10 ppm/ °C.

6.4.2 External Reference and Internal Buffer

To improve temperature drift performance, an external reference source can be used with the internal buffer. The external reference source output is connected to REFIN and is output at the REF pin after passing through the internal buffer. The external reference source can be used with the internal buffer with or without the temperature sensor enabled. See Table 4 for register details. With the internal buffer enabled, the internal buffer is in unity gain mode and is limited to 4.096 V input/output.

The internal reference buffer is useful in multi-converter applications where a buffer is often required. A low power reference can also be used since the internal buffer provides the performance required to drive the GD30AD3382 SAR architecture.

6.4.3 Reference Source Decoupling Capacitor

Whether using an internal or external reference source, the GD30AD3382 voltage reference output/input (REF pin) has a dynamic input impedance and therefore needs to be driven by a low impedance source with effective decoupling capacitance between the REF and GND pins. This decoupling capacitance depends on the choice of voltage reference source, but is typically composed of low ESR capacitors connected to REF and GND with minimal parasitic inductance. When using the internal reference, a 10 μF (X5R, 1206 size) ceramic chip capacitor is recommended.

The layout location of the reference source's decoupling capacitor is also important to the performance of Layoutsection. Place the decoupling capacitor on the same side of the ADC's REF pin and use wide PCB traces. GND is also connected to the reference decoupling capacitor with the shortest distance and to the analog ground through several vias.

If desired, smaller reference source decoupling capacitor values as low as 2.2 μF can be used with minimal impact on performance, especially on DNL.

6.4.4 Powering the ADC from a Voltage Reference

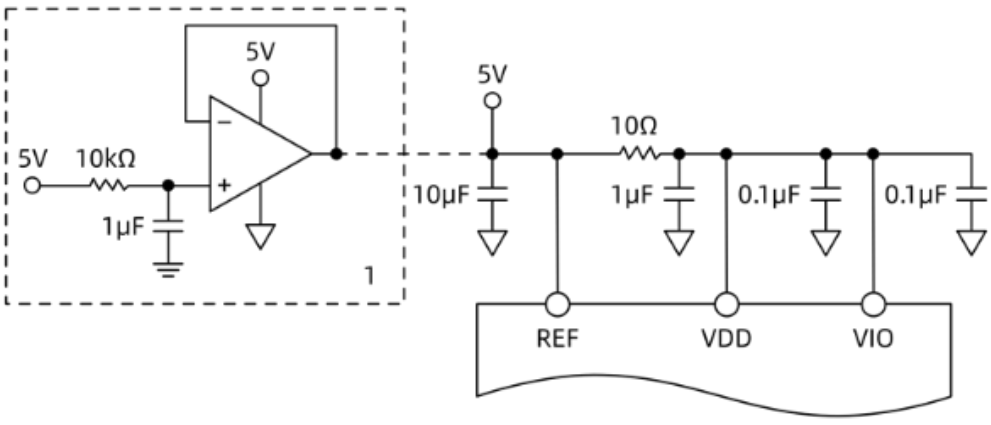


Figure 20. Application Circuit Example

1. REFERENCE buffers and filters .

7 Digital Interface

The GD30AD3382 uses a simple 4-wire interface that is compatible with SPI, MICROWIRE™, QSPI™, digital hosts, and DSPs.

The interface uses the CNV, DIN, SCK, and SDO signals and allows the CNV that initiates the conversion to be independent of the readback time. This is useful in low jitter sampling or synchronous sampling applications.

A 14-bit register, CFG[13:0], configures the ADC channels to be converted, reference selection, and other components, as detailed in *Configuration Register CFG* section.

When CNV is low, read/write can occur during sampling and conversion, details of which are described in the following sections. CFG is updated on the first 14 SCK rising edges (16 if busy mode is selected), and the conversion results are output sequentially on the first 15 (first 16 if busy indication mode is selected) falling edges of SCK. If CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word associated with the conversion result, with the CFG MSB following the LSB of the conversion result.

It is recommended to use discontinuous SCK because the device is selected when CNV is low and writing a new configuration word and outputting data begins when SCK is active.

Note that the timing diagrams below show the activity of digital signals (SCK, CNV, DIN, SDO) during conversion. However, to prevent performance degradation, digital activity should only occur before the safe data read and write time t_{DATA}. If data is read or written between t_{DATA} and t_{CONV}, the conversion result may be corrupted. The user must configure the GD30AD3382 and initiate a busy indication (if necessary) before t_{DATA}. If there is a toggle of SCK or DIN at the sampling moment, it may corrupt the sampling. Therefore, it is recommended to keep the digital pins quiet and use discontinuous SCK within 30ns before and 10ns after the rising edge of CNV to prevent performance degradation.

7.1 Read/Write on Conversion, Fast Host

When reading or writing during the nth conversion, the result of the last (n-1) conversion is read, and the CFG written in will be used by the next (n+1) conversion.

CNV changes from low to high to trigger the ADC conversion, and then CNV needs to be pulled low to perform read and write operations during the conversion.

Before t_{DATA}, the read and write operations must be completed. Due to the limited time, the host must use a fast SCK. The required SCK frequency calculation formula is:

$$f_{sck} \geq \frac{Number\_SCK\_Edges}{t_{DATA}} \quad (1)$$

Between t_{DATA} and t_{CONV} the digital pins must not be active, otherwise sensitive bits may be corrupted.

7.2 Read/Write after Conversion

After the (n-1)th conversion, or during the nth sampling, the result read is the (n-1)th conversion result, and the configuration written is for the (n+1)th conversion.

For maximum throughput rates, the only timing constraints are the points in time during t_{ACQ} when the re ad and write operations occur. For slower throughput rates, the timing constraints are determined by the

throughput required by the user, and the host is free to run at any speed. Therefore, for slow hosts, dat a access must occur during the acquisition phase.

7.3 Read and Write During Conversion

When reading or writing during conversion, data transfer starts from the current (n) sampling phase and crosses to the conversion (n) phase. The result read is the result of the previous (n−1) conversion, and the value written to the CFG register is used for the next (n+1) acquisition and conversion.

Similar to reads/writes during conversion, reads/writes can only occur before t_{DATA}. For maximum throughput, the only timing constraint is the point in time during t_{ACQ} when the read and write operations occur.

For slow throughput rates, the time constraints are determined by the throughput required by the user, and the host is free to run at any speed. Similar to reading and writing during acquisition, for slow hosts, data access must occur during the sampling phase and add additional time to the conversion. It is important to note that reading data across conversions requires CNV to be pulled high to start a new conversion. Data access is not allowed when CNV is high. Therefore, the host must perform two data accesses when using this method.

7.4 Configuration Register CFG

The GD30AD3382 uses a 14-bit configuration register (CFG[13:0]) as shown in Table 4. CFG contains detailed input configuration, conversion channels, single-pole filter bandwidth, reference source, and channel sequencer. The device latches the CFG register value through 14 SCK rising edges (MSB first). The CFG register can be written during conversion, during sampling, or across sampling/conversion periods, and is updated at the end of conversion. There is always a deep delay when writing to the CFG register. Note that at power-on, the CFG register is undefined and two dummy conversions are required to update the register. If you want to use the factory preset CFG register value, keep DIN high for two conversions. In this way, CFG[13:0] = 0x3FFF. This sets the GD30AD3382 as follows:

- IN[7:0] single-ended, referenced to GND, sequenced in order
- Single-pole filter uses full bandwidth
- Internal reference/temperature sensor disabled, buffer enabled
- Enable sequencer
- Do not read back the CFG register

The following table summarizes the configuration register bit details. See *Operation* section for more details.

Table 4.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC	INCC	INCC	INx	INx	INx	BW	REF	REF	REF	SEQ	SEQ	RB

Table 5. Configuration Register Description

BIT (S)	NAME	DESCRIPTION
[13]	CFG	Configuration updates. 0 = Keep current configuration. 1 = Overwrite the contents of the register.
[12:10]	INCC	Input channel configuration. Select Pseudo Differential, Pseudo Differential, Input

BIT (S)	NAME	DESCRIPTION			
		Pair, Single-Ended, or Temperature Sensor. See *Input Configuration* section.			
		Bit 12	Bit 11	Bit 10	Function
		0	0	X[1]	Bipolar differential pairs; INx− referenced to VREF/2 ± 0.1 V.
		0	1	0	Bipolar; INx referenced to COM = VREF/2 ± 0.1 V.
		0	1	1	Temperature sensor.
		1	0	X[1]	Unipolar differential pairs; INx− referenced to GND ± 0.1 V.
		1	1	0	Unipolar, IN0 to IN7 referenced to COM = GND ± 0.1 V (GND sense).
		1	1	1	Unipolar, IN0 to IN7 referenced to GND.
[9:7]	INx	Binary input channel selection.			
		Bit 9	Bit 8	Bit 7	channel
		0	0	0	IN0
		0	0	1	IN1
		…	…	…	…
		1	1	1	IN7
[6]	BW	Low-pass filter selects bandwidth. 0 = 1/4 of full bandwidth, use additional series resistors to further limit bandwidth noise. Maximum throughput must also be reduced to 1/4. 1 = full bandwidth.			
[5:3]	REF	Reference source/buffer selection. Selects internal, external, and externally buffered reference voltages and enables the on-chip temperature sensor. See *Voltage Reference Output/Input* section.			
		Bit 5	Bit 4	Bit 3	function
		0	0	0	Not use
		0	0	1	Internal reference enabled, REF = 4.096V output, temperature sensor enabled.
		0	1	0	External reference voltage source enabled, temperature sensor enabled
		0	1	1	External reference voltage source enabled, internal buffer enabled, temperature sensor enabled
		1	0	0	Not use
		1	0	1	Not use
		1	1	0	External reference enabled, temperature sensor disabled
		1	1	1	External reference enabled, internal buffer enabled, temperature sensor disabled
[2:1]	SEQ	Channel sequencer. Allows channels to be scanned from IN0 to IN[7:0]. See			

BIT (S)	NAME	DESCRIPTION		
		Sequencer section.		
		Bit 2	Bit 1	function
		0	0	Disable Sequencer
		0	1	Update configuration during sequence
		1	0	Scan IN0 to IN[7:0] (set in CFG[9:7]), then scan the temperature.
		1	1	Scan IN0 to IN[7:0] (set in CFG[9:7]).
0	RB	Read back the CFG register 0 = Read back the current configuration at the end of data 1 = Do not read back configuration		

1. X means don't care.
2. The temperature sensor is always enabled when the internal band gap reference is enabled. See *Voltage Reference Output/Input* section.

7.5 Universal Timing, No Busy Indication

Figure 21 details the timing for all three modes : read/write during conversion, read/write after conversion, and read/write across conversion. CFG and data read are updated at the end of conversion (EOC). At the end of conversion (EOC), if CNV is high, the busy indicator is turned off.

As mentioned earlier, data access occurs before the safe data read and write time $t_{DATA.}$ If the complete CFG word is not written before EOC, it will be discarded and the current configuration will be retained. If the conversion result is not completely read out before EOC, the new conversion result will also be updated on SDO. See the detailed timing diagram below.

When CNV goes low after EOC, SDO is driven to MSB by high impedance. The falling SCK edge starts timing with MSB − 1.

If you use the SPI interface, SCK can be high or low during idle time, depending on the configuration of the clock polarity (CPOL) and phase (CPHA). A simple solution is to use CPOL = CPHA = 0, as shown in the figure below, SCK idle time is low.

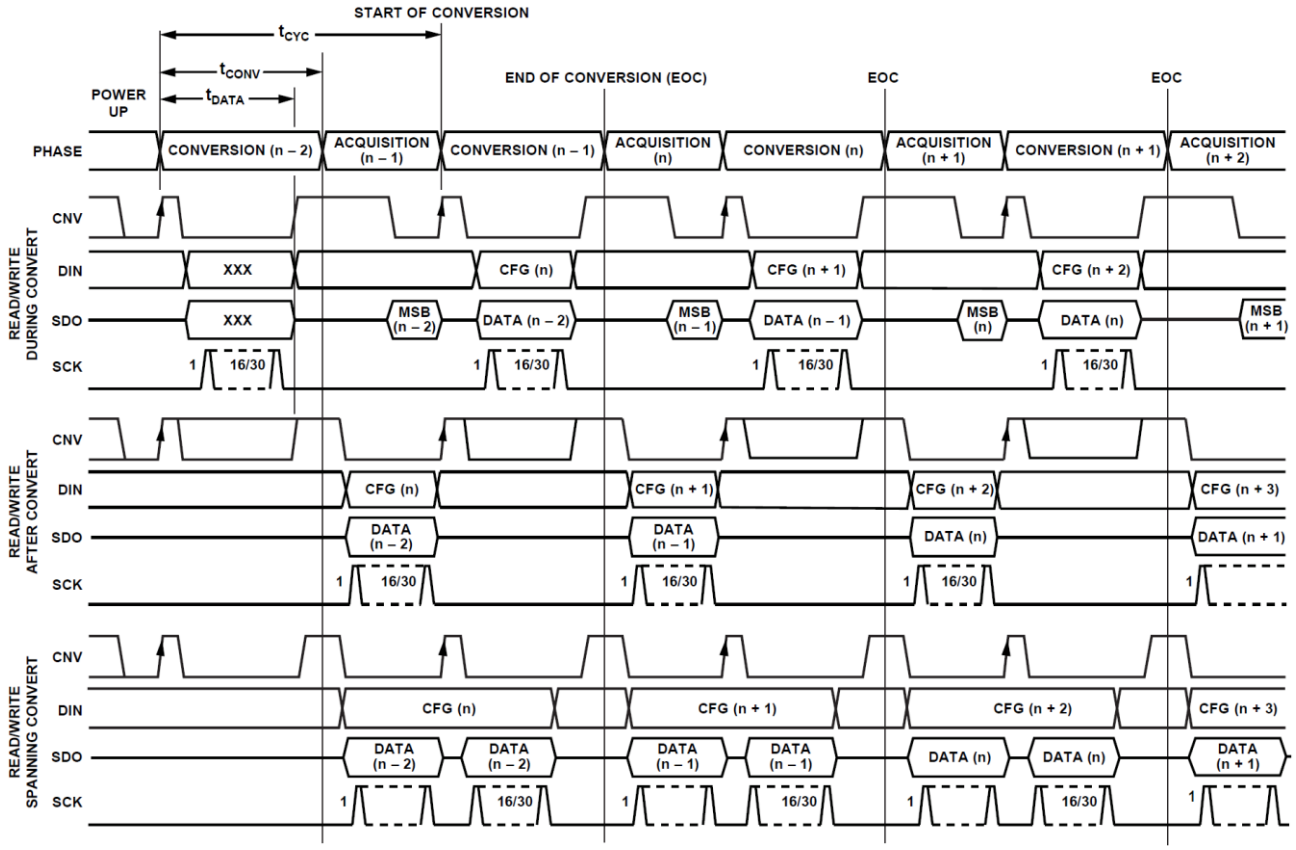


Figure 21. GD30AD3382 General Interface Timing Diagram, No Busy Indication

1. CNV must be high before the end of CONVERSION (EOC) to avoid a busy indication. A total of 16 SCK falling edges are required to restore SDO to the High-Z state. If CFG is read back, a total of 30 SCK falling edges are required before SDO returns to the High-Z state.

7.6 General Timing, with Busy Indication

Figure 22 details the timing for all three modes: read and write during conversion, read and write after conversion, and read and write across conversion. The CFG and result data are updated at the end of conversion (EOC). As mentioned earlier, data access must occur before the safe data read and write time t_{DATA}. If the complete CFG word is not written before EOC, it is discarded and the current configuration is retained.

At EOC, if CNV is low, the busy indication is enabled. To correctly generate the busy indication, the host must generate at least 17 SCK falling edges to return SDO to the High-Z state.

Unlike the case without busy indication, if the conversion result is not completely read out before EOC, the last 1 bit of data will be retained. If this 1 bit is 0, SDO will remain at a low level, and the busy indication signal cannot be generated. Because before the busy indication signal is generated, SDO needs to remain High-Z or high level in order to generate a change from high to low, thereby inputting an interrupt signal to the host. For example, for an 8-bit SPI host interface, if the SPI host sends 16 SCKs, the LSB data will remain on SDO after the last SCK, which requires more SCKs. For this SPI host, 24 SCKs should be sent for one operation.

SCK can be high or low during idle time, depending on the configuration of clock polarity (CPOL) and phase (CPHA). A simple solution is to use CPOL = CPHA = 1 (not shown in the figure), and SCK remains high during idle time.

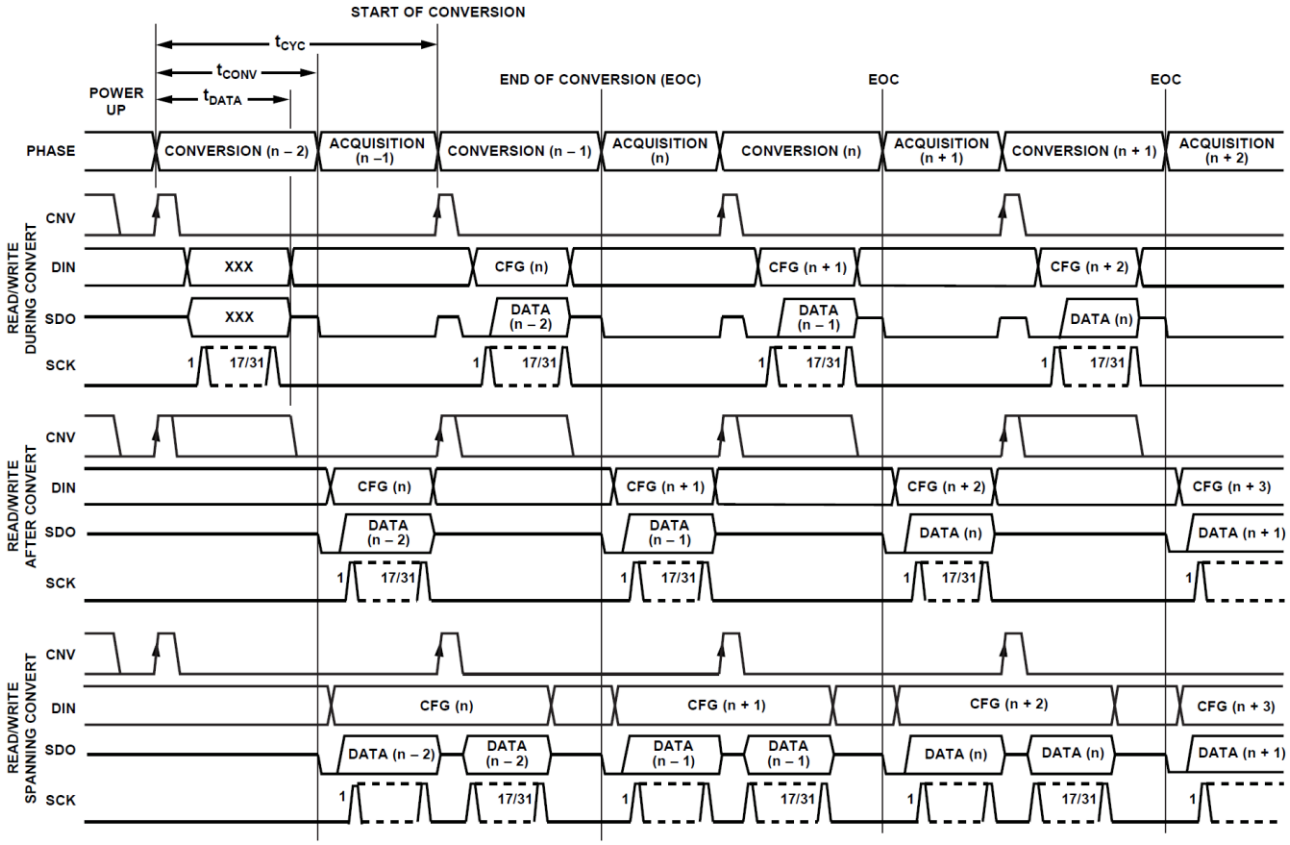


Figure 22. GD30AD3382 General Interface Timing Diagram with Busy Indication

1. CNV must be high before the end of CONVERSION (EOC) to avoid a busy indicator. A total of 17 SCK falling edges are required to restore SDO to a High-Z value. If CFG is read, a total of 31 SCK falling edges are required to return SDO to a High-Z state.

7.7 Read and Write Across Transitions, No Busy Indication

This mode is used when the GD30AD3382 is connected to any host via SPI, serial port or FPGA. The connection diagram is shown in Figure 23, and the corresponding timing is given in Figure 24. For SPI, the host must use CPHA=CPOL= 0. Figure 24 shows the timing diagram for read and write across transitions, which covers the three modes of the digital interface. For this mode, the host must generate the data transfer timing based on the transition time. For interrupt-driven transmission, please refer to *Read and Write Across Conversions, with Busy Indication*, where busy indication is used.

On the rising edge on CNV, the ADC starts converting, SDO goes High-Z, and ignores the data on DIN. Once a conversion starts, it continues until the conversion is complete, regardless of the state of CNV during the period. CNV must return to a high state before the safe data transfer time t_{DATA} and remain high until after t_{CONV} to avoid generating a busy indicator signal.

After the conversion is completed, the GD30AD3382 enters the acquisition phase. After t_{CONV}, the host pulls CNV low and the MSB data is output on SDO. If CFG needs to be updated, the host also sends the MSB of CFG at this time. During the CNV low level, CFG is updated and data is read back. The device captures CFG on the first 14 SCK rising edges and outputs the conversion results starting from MSB − 1 on the first 15 SCK falling edges. Data access must occur before the safe data read and write time t_{DATA}. If the complete CFG word is not written

before EOC, it will be discarded and the current configuration will be retained. If the 16-bit conversion result is not read before t_{DATA}, the conversion result will be lost. SDO data is valid on both the rising and falling edges of SCK. Although data can be captured on the SCK rising edge, using the SCK falling edge to capture data can increase the reading rate. After 16 (or 30) SCK falling edges, or when CNV rises (whichever occurs first), SDO returns to high impedance.

If the CFG readback feature is enabled, the CFG associated with the conversion result will be output MSB first after the LSB of the conversion result. A total of 30 SCK falling edges are required to return SDO to the High-Z state.

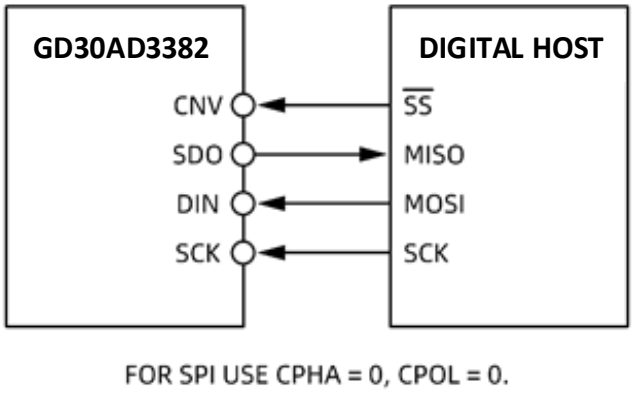


Figure 23. GD30AD3382 without Busy Indication Connection Diagram

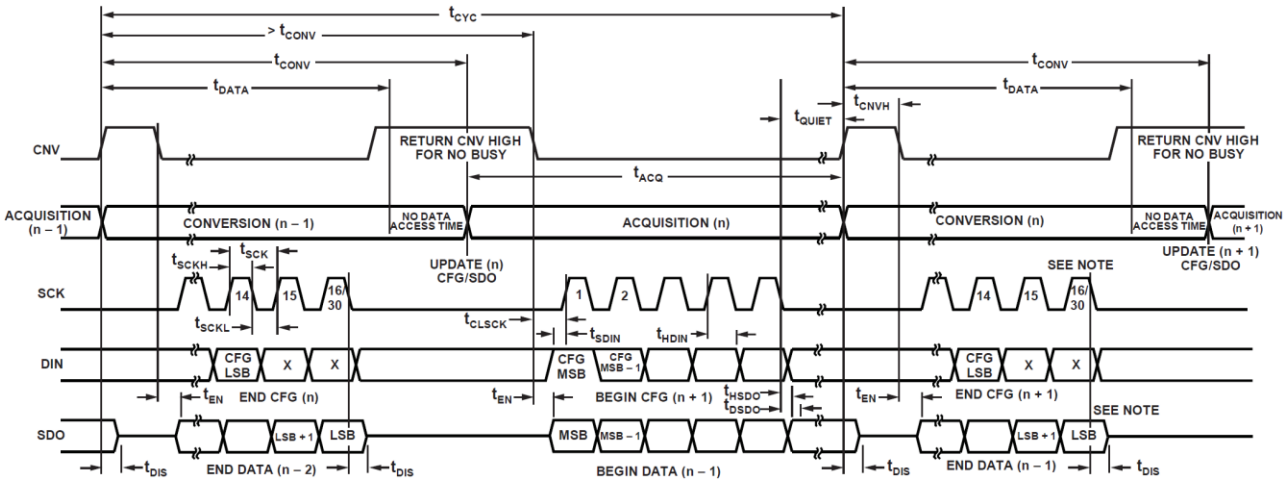


Figure 24. GD30AD3382 Serial Timing Interface, No Busy Indicator

1. The LSB is the least significant bit of the conversion result or the least significant bit of the configuration register CFG(n - 1).
   15th SCK falling edge: LSB of conversion result.
   29th SCK falling edge: LSB of configuration register.
   At the 16th or 30th SCK falling edge, SDO changes to high impedance.
2. The data-free access time is the time difference between t_{CONV} and t_{DATA}.

7.8 Read and Write Across Conversions, with Busy Indication

When GD30AD3382 uses this mode, the connection diagram is shown in Figure 25, and the corresponding timing is given in Figure 26. For the SPI master, use the CPHA = CPOL= 1 mode. Figure 26 shows the transition-crossing

read and write timing, which covers all three modes introduced in the digital interface section.

On the rising edge on CNV, the ADC starts converting, SDO goes to High-Z, and ignores the data on DIN. Once the conversion starts, it continues until the conversion is complete, regardless of the state of CNV during the period. CNV goes to the low state before t_{DATA} to generate a busy indicator. Before the conversion is complete, SDO remains in a high-impedance state and is pulled to VIO by the pull-up resistor; after the conversion is complete, SDO goes from high to low. This can send an interrupt to the host so that the host can start transmitting data.

After the conversion is completed, GD30AD3382 enters the acquisition phase. If CFG needs to be updated, the host sends the MSB of CFG at this time, and CFG is updated and data is read back during the CNV low level. The device captures CFG on the first 14 SCK rising edges and outputs the conversion results starting from the MSB on the first 16 SCK falling edges. Data access must occur before the safe data read and write time t_{DATA}. If the complete CFG word is not written before EOC, it will be discarded and the current configuration will be retained. If the 16-bit conversion result is not read before t_{DATA}, the conversion result will be lost. SDO data is valid on both the rising and falling edges of SCK. Although data can be captured on the SCK rising edge, using the SCK falling edge to capture data can increase the reading rate. After 17 SCK falling edges, SDO returns to high impedance. Note that if there is no 17th SCK falling edge and the LSB of the conversion result is 0, the busy indication signal cannot be generated normally. If the CFG readback function is enabled, the CFG associated with the conversion result will be output in an MSB-first manner after the LSB of the conversion result. A total of 31 SCK falling edges are required to restore SDO to the High-Z state.

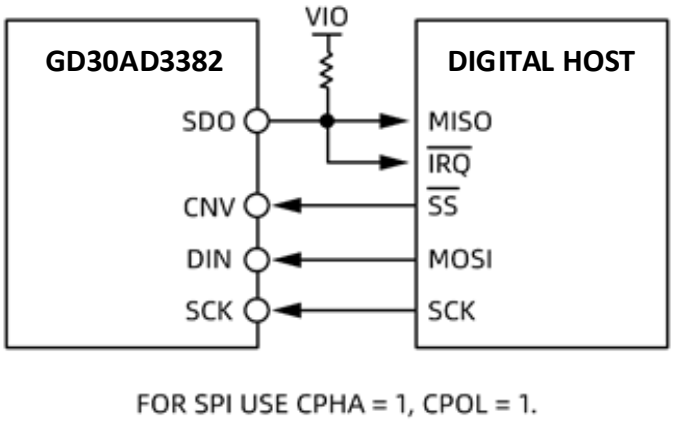


Figure 25. GD30AD3382 with Busy Indication Connection Diagram

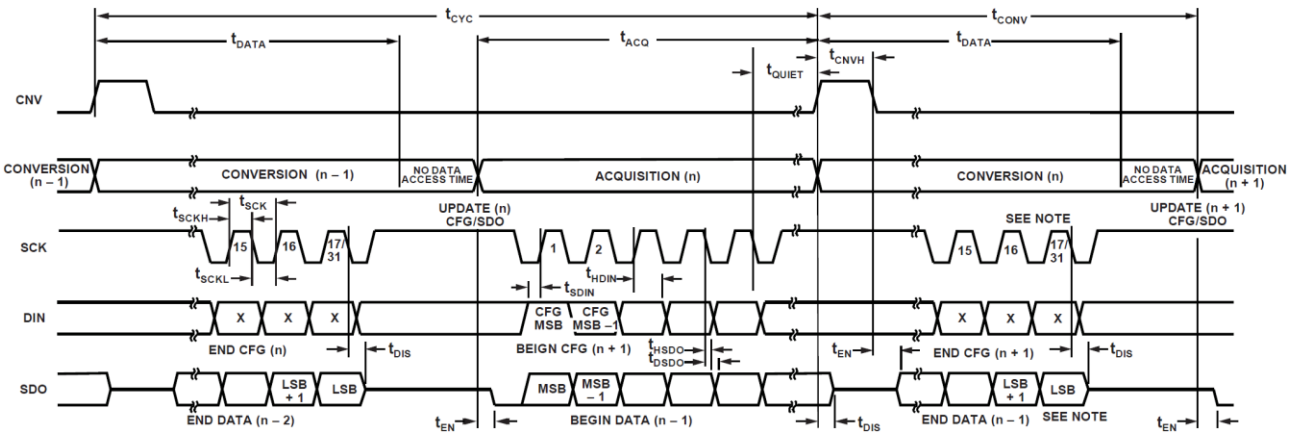


Figure 26. GD30AD3382 Serial Timing Interface with Busy Indication

1. The LSB is the least significant bit of the conversion result or the least significant bit of the configuration register CFG(n - 1).

   16th SCK falling edge: LSB of conversion result.

   30th SCK falling edge: LSB of configuration register.

   At the 17th or 31st SCK falling edge, SDO changes to high impedance.
2. The data-free access time is the time difference between t_{CONV} and t_{DATA}.

7.9 Channel Sequencer

The GD30AD3382 includes a channel sequencer for scanning channels in a repetitive manner. Channel scanning can be single-ended or in pairs, with or without a temperature sensor.

The sequencer starts with IN0 and ends with IN[7:0] set in CFG[9:7]. For paired channels, the pairing of the channels depends on the last channel set in CFG[9:7]. Note that in sequencer mode, the positive input channels of paired channels are always assigned to even channels (IN0, IN2, IN4, and IN6), and the negative input channels are always assigned to odd channels (IN1, IN3, IN5, and IN7). For example, setting CFG[9:7] = 110 or 111 scans IN0, IN2, IN4, and IN6 for all positive inputs.

CFG[2:1] enables the sequencer. After the CFG register is updated, DIN must be kept low until the 13th bit is read out, otherwise the CFG register starts updating again.

Note that some bits in the CFG register can be changed while the sequencer is operating. However, if you change CFG[11] (pair or single channel) or CFG[9:7] (last channel in the sequence), the sequence will be reinitialized and start converting from IN0 (or IN0/IN1 pair) after the CFG register is updated.

The following figure details the timing for all three modes without a busy indication. The sequencer can also be used with a busy indication and details of these timings can be found in the *General Timing, with Busy Indication* section and *Read and Write Across Conversions, with Busy Indication* section.

For sequencer operation, the CFG register must be set in phase (n-1) after power-up. In phase (n), the sequencer settings take effect and IN0 is sampled. The first valid conversion result is available in phase (n+1). After the last channel conversion set in CFG[9:7] is completed, the internal temperature sensor data is output (if enabled), and then IN0 is sampled.

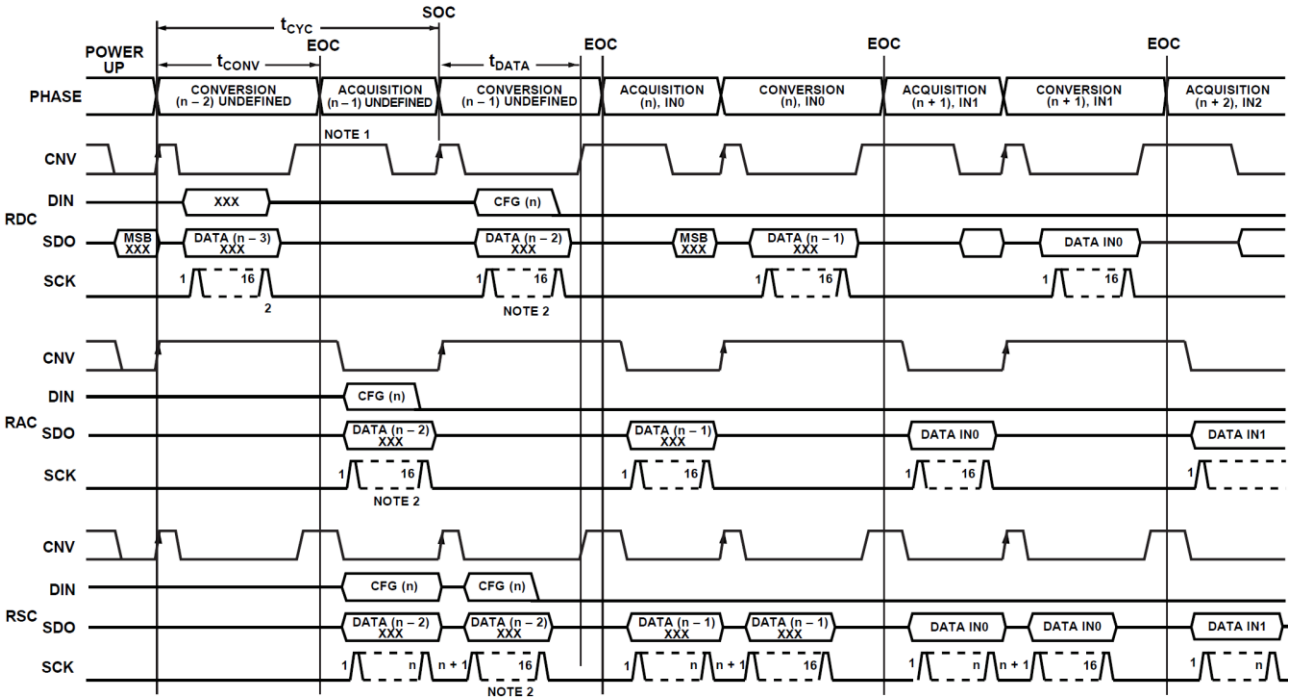


Figure 27. Generic Channel Sequencer Timing without Busy Indicator

1. CNV must be pulled high before the CONVERSION is complete to avoid a busy indication.
2. A total of 16 SCK falling edges are required to return SDO to high impedance. If readback CFG is enabled, a total of 30 SCK falling edges are required to return SDO to high impedance.

8 Application Information

8.1 Layout

The PCB design of GD30AD3382 must separate the analog and digital GND and confine them to certain areas of the circuit board. In the pinout of GD30AD3382, all analog signals are on the left and all digital signals are on the right. This pinout arrangement can simplify the design.

Avoid running digital traces directly under the GD30AD3382, because noise will couple to the GD30AD3382 unless the layer directly below the GD30AD3382 is shielded with GND. Fast switching signals, such as CNV or clock, cannot run near analog signal paths. Avoid crosstalk between digital and analog signals.

Use at least one ground plane. It can be common or split between the digital and analog sections. In the latter case, connect the planes underneath the GD30AD3382.

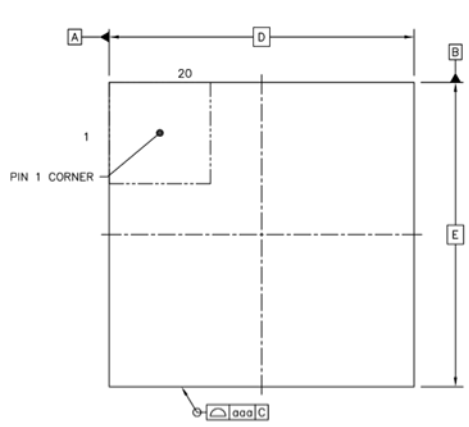
The GD30AD3382 voltage reference input REF pin has a dynamic input impedance and must be decoupled by a small parasitic inductance. By placing the reference source decoupling ceramic capacitor close to the layout, ideally REF and GND are connected by wide, short, low-impedance traces.

Finally, the decoupling capacitors for power supplies VDD and VIO, usually 100nF ceramic capacitors, are placed as close to the pins as possible and connected with short and wide traces to provide a low impedance path and reduce the impact of glitch noise on the power supply line.

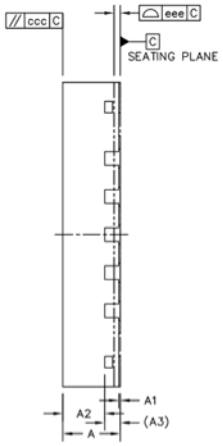
9 Packaging Information

9.1 Outline Dimensions

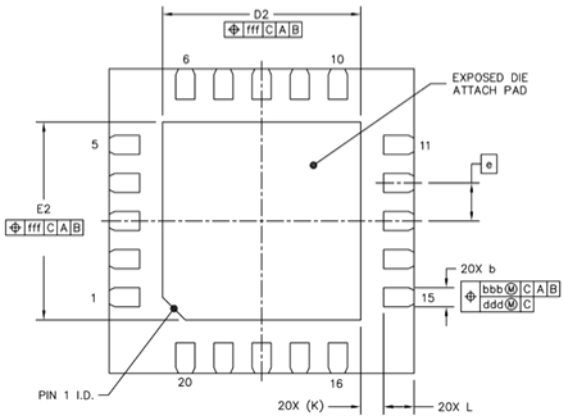
QFN-20 Dimensions



TOP VIEW



SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.5	2.6	2.7
	Y	E2	2.5	2.6	2.7
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

NOTES:

1. All dimensions are in millimeters (mm).
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to Table 1. *QFN 20 size (mm)*.

Table 1. QFN 20 size (mm)

SYMBOL	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2		0.55	
A3		0.203 REF	
b	0.2	0.25	0.3
D		4 BSC	
E		4 BCS	
e		0.5 BSC	
D2	2.5	2.6	2.7
E2	2.5	2.6	2.7
L	0.3	0.4	0.5
K		0.3 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.1	
ddd		0.05	
f		0.1	

10 Ordering Information

Order Model	Package Type	ECO Plan	Packaging Type	MOQ	Op Temp (°C)
GD30AD3382FUTR-I02	QFN20	Green	Tape & Reel	3000	−40°C to +105°C
GD30AD3382FUTR-I05	QFN20	Green	Tape & Reel	3000	−40°C to +105°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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