16-Channel DAS with 16-Bit、Bipolar Input、Dual-Channel Simultaneous Sampling ADC

1 Features

- 16-channel, dual-way, synchronous sampling input
- Independently selectable channel input ranges
  - True bipolar: ±10 V, ±5 V, ±2.5 V
- 5 V single analog supply, V_{DRIVE} supply voltage: 2.3 V to 3.6 V
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - First order anti-aliasing analog filter
  - On-chip precision voltage reference and reference voltage buffer
  - Dual-channel 16-bit Successive Approximation Register (SAR) ADC
  - Throughput rate: 2×1 MSPS
  - Oversampling capability provided by digital filter
  - Flexible sequencer, supporting burst mode
- Flexible parallel/serial interface
  - SPI/QSPI/MICROWIRE/DSP compatible
- Hardware/Software Configuration
- performance
  - Signal-to-Noise Ratio (SNR): 90.5 dB (1 MSPS)
  - Total Harmonic Distortion (THD): -103 dB
  - ±1 LSB INL (typ), ±0.99 LSB DNL (max)
  - 7 kV ESD rating on analog input channels
- On-chip self-test function
- 80-pin LQFP package

2 Application

- Power line monitoring
- Protection relay
- Multiphase Motor Control
- Instrumentation and control systems
- Data Acquisition System (DAS)

3 Description

The GD30AD33G0 is a 16-bit DAS that supports dual-channel simultaneous sampling of 16 channels. The GD30AD33G0 operates from a single 5 V power supply and can handle ±10 V, ±5 V, and ±2.5 V true bipolar input signals while each pair of channels can sample at up to 1MSPS throughput and 90.5 dB SNR.

The GD30AD33G0 input clamp protection circuit can withstand voltages up to ±25 V. Regardless of the sampling frequency, the analog input impedance of the GD30AD33G0 is 1 MΩ. It operates in a single-supply mode with on-chip filtering and high input impedance, eliminating the need for a driver op amp and external bipolar power supply.

The device integrates analog input clamp protection, a dual 16-bit charge redistribution SAR analog-to-digital converter (ADC), a flexible digital filter, 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

GD30AD33G0 is compatible with Serial Peripheral Interface (SPI)/QSPI/DSP/MIC-ROWIRE.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE(NOM)
GD30AD33G0	LQFP80	14.00mm x 14.00mm

1. For packaging details, see *Packaging Information* section.

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4 Device Overview

4.1 Pinout and Pin Assignment

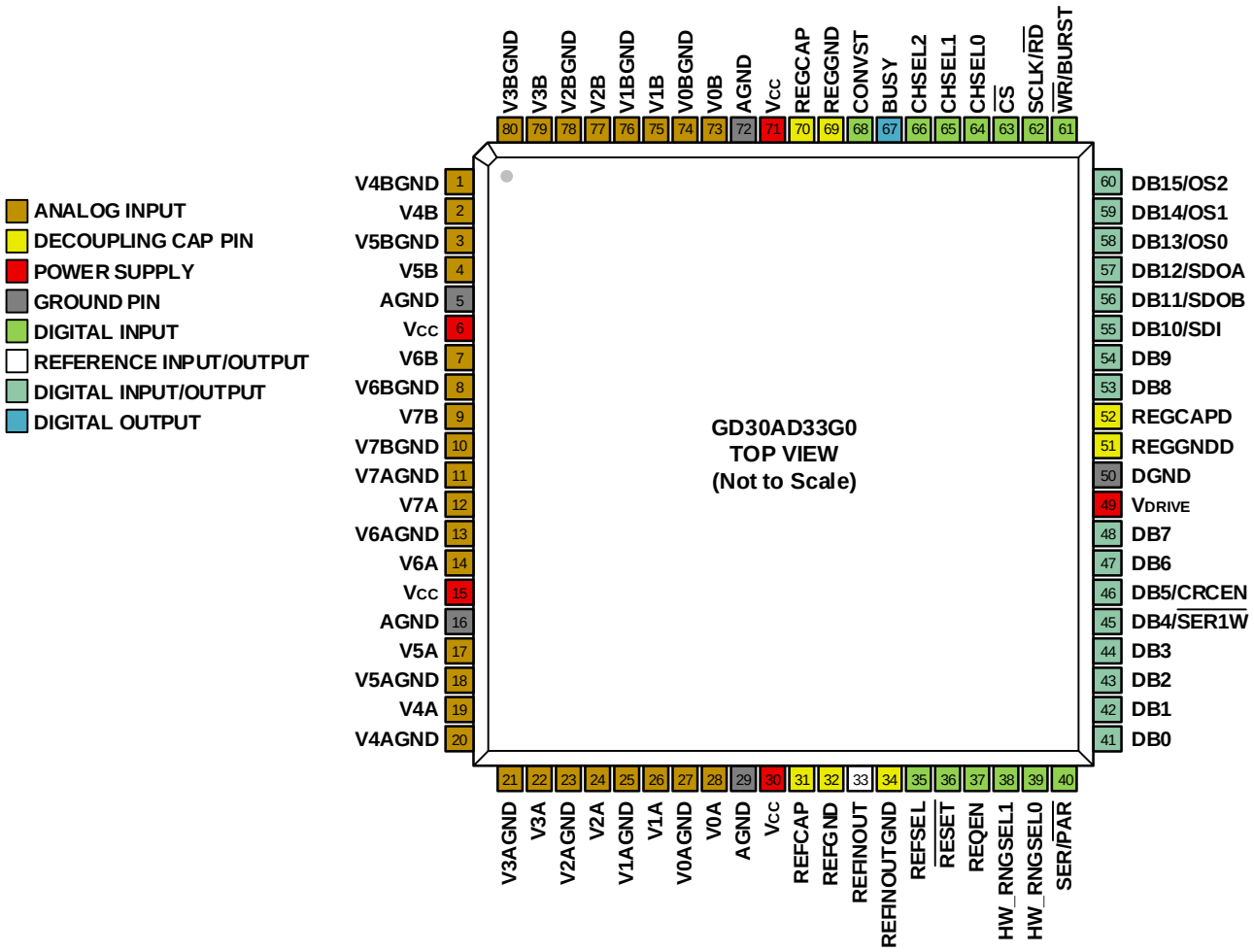


Figure 1. Pin Configuration

4.2 Pin Description

PINS		PIN TYPE[1]	FUNCTION
NAME[2]	NUM		
V4BGND	1	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V4B.
V4B	2	AI	Channel 4 Analog Input, ADC B.
V5BGND	3	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V5B.
V5B	4	AI	Channel 5 Analog Input, ADC B.
AGND	5, 16, 29, 72	P	Analog power ground pin.
V_{CC}	6, 15, 30, 71	P	Analog supply voltage, 4.7 V to 5.25 V. This is the supply voltage for the internal front-end amplifier and ADC core. These pins should be decoupled to AGND with 0.1 µF and 10 µF parallel capacitors.
V6B	7	AI	Channel 6 Analog Input, ADC B.
V6BGND	8	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V6B.
V7B	9	AI	Channel 7 Analog Input, ADC B.
V7BGND	10	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V7B.
V7AGND	11	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V7A.
V7A	12	AI	Channel 7 Analog Input, ADC A.
V6AGND	13	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V6A.
V6A	14	AI	Channel 6 Analog Input, ADC A.
V5A	17	AI	Analog input V5A.
V5AGND	18	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V5A.
V4A	19	AI	Analog input V4A.
V4AGND	20	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V4A.
V3AGND	21	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V3A.
V3A	22	AI	Channel 3 Analog Input, ADC A.
V2AGND	23	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V2A.
V2A	24	AI	Channel 2 Analog Input, ADC A.
V1AGND	25	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V1A.
V1A	26	AI	Channel 1 Analog Input, ADC A.

PINS		PIN TYPE[1]	FUNCTION
NAME[2]	NUM		
V0AGND	27	AIGND	Analog input ground pin. This pin corresponds to the analog input pin V0A.
V0A	28	AI	Channel 0 Analog Input, ADC A.
REFCAP	31	CAP	Reference Voltage Buffer Output Force/Sense Pin. Decouple this pin to AGND with a low effective series resistance (ESR), 10 µF, X5R ceramic capacitor as close to the REFCAP pin as possible. The voltage on this pin is typically 4.096V.
REFGND	32	CAP	Reference voltage ground pin. This pin should be connected to AGND.
REFINOUT	33	REF	Reference Voltage Input/Reference Voltage Output. When the REFSEL pin is set to logic high, this pin provides the 2.5V on-chip reference voltage for external use. Alternatively, the REFSEL pin can be set to logic low to disable the internal reference voltage and apply a 2.5V external reference voltage to this input. Decoupling of this pin is required whether using an internal or external reference voltage. A 100nF X8R capacitor should be connected between the REFINOUT pin and REFINOUTGND as close to the REFINOUT pin as possible. If an external reference voltage source is used, a 10kΩ series resistor should be connected to this pin to limit the reference signal bandwidth.
REFINOUTGND	34	CAP	Reference voltage input and reference voltage output ground pins.
REFSEL	35	DI	Internal/External Reference Select Input. REFSEL is a logic input. If this pin is set to logic high, the internal reference mode is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference must be applied to the REFINOUT pin. When full reset is released, the signal state is latched and another full reset is required to reconfigure.
$\overline{\text{RESET}}$	36	DI	Reset Input. Full and partial reset options are available. The type of reset is determined by the $\overline{\text{RESET}}$ pulse length. When $\overline{\text{RESET}}$ held low, the device is placed in shutdown mode. See *Reset Function* section for details.
SEQEN	37	DI	Channel Sequencer Enable Input (Hardware Mode Only). When SEQEN is tied low, the sequencer is disabled. When SEQEN is high, the sequencer is enabled (limited functionality in hardware mode). See the Sequencer. When full reset is released, the signal state is latched and another full reset is required to reconfigure. In software mode, this pin must be connected to DGND.
HW_RNGSEL1 HW_RNGSEL0	38, 39	DI	Hardware/Software Mode Select, Hardware Mode Range Select Input. Hardware/Software Mode Select is latched on full reset. Range selection in Hardware Mode is not latched. HW_RNGSELx = 00: Software mode; GD30AD33G0 is configured via

PINS		PIN TYPE[1]	FUNCTION
NAME[2]	NUM		
			software registers. HW_RNGSELx = 01: Hardware mode; analog input range is ±2.5 V. HW_RNGSELx = 10: Hardware mode; analog input range is ±5 V. HW_RNGSELx = 11: Hardware mode; analog input range is ±10 V.
SER/$\overline{PAR}$	40	DI	Serial/Parallel Interface Select Input. Logic Input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. When full reset is released, the signal state is latched and another full reset is required to reconfigure.
DB0, DB1, DB2, DB3	41, 42, 43, 44	DO/DI	Parallel output/input data bit 0 to data bit 3. In parallel mode, these pins are the output/input parallel data bits DB7 to DB0. See the *Parallel Interface* section for details. In serial mode, these pins must be connected to DGND.
DB4/$\overline{SER1W}$	45	DO/DI	Parallel Output/Input Data Bit 4/Serial Output Select. In Parallel mode, this pin acts as a three-state parallel digital output/input pin. See the *Parallel Interface* section for details. In serial mode, this pin determines whether the serial output works on SDOA and SDOB, or only on SDOA. When $\overline{SER1W}$ is low, the serial output only works on SDOA; when $\overline{SER1W}$ is high, the serial output works on SDOA and SDOB. When the full reset is released, the signal state is latched and another full reset is required to reconfigure.
DB5	46	DO/DI	Parallel Output/Input Data Bit 5. In parallel mode, this pin acts as a three-state parallel digital input/output. In software mode, this pin must be connected to DGND.
DB6, DB7	47, 48	DO/DI	Parallel Output/Input Data Bit 6 and Data Bit 7. These pins act as three-state parallel digital input/outputs when SER/$\overline{PAR}$ = 0. See the *Parallel Interface* section for details. In serial mode, when SER / $\overline{PAR}$ = 1, these pins must be connected to DGND.
V_{DRIVE}	49	P	Logic Power Input. The supply voltage at this pin determines the operating voltage of the logic interface. The nominal supply at this pin is the same as the host interface supply. This pin should be decoupled with a 0.1 µF and 10 µF parallel capacitor.
DGND	50	P	Digital ground. This pin is the ground reference point for all digital circuits on the GD30AD33G0 . The DGND pin must be connected to the DGND plane of the system.
REGGNDD	51	CAP	Connect to the ground of the digital low dropout (LDO) regulator at REGCAPD (Pin 52).
REGCAPD	52	CAP	Decoupling capacitor pin for the internal digital regulator voltage output. This output pin should be independently decoupled to REGGNDD with a 10 µF capacitor. The voltage at this pin is typically 1.89V.

PINS		PIN TYPE[1]	FUNCTION
NAME[2]	NUM		
DB8, DB9	53, 54	DO/DI	Parallel Output/Input Data Bit 9 and Data Bit 8. These pins act as three-state parallel digital input/outputs when SER/$\overline{PAR}$ = 0. See the *Parallel Interface* section for details. In serial mode, when SER / $\overline{PAR}$ = 1, these pins must be tied to DGND.
DB10/SDI	55	DO/DI	Parallel Output/Input Data Bit DB10/Serial Data Output. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state parallel digital input/output. See the *Parallel Interface* section for details. In hardware serial mode, this pin should be connected to DGND. In serial mode, when SER / $\overline{PAR}$ = 1, this pin serves as the data input for the SPI interface.
DB11/SDOB	56	DO/DI	Parallel Output/Input Data Bit 11/Serial Data Output B. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state parallel digital input/output. See the *Parallel Interface* section for details. In serial mode, when SER / $\overline{PAR}$ = 1, this pin functions as SDOB, outputting serial conversion data.
DB12/SDOA	57	DO/DI	Parallel Output/Input Data Bit 12/Serial Data Output A. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state parallel digital input/output. See the *Parallel Interface* section for details. In serial mode, when SER / $\overline{PAR}$ = 1, this pin functions as SDOA, outputting serial conversion data.
DB13/OS0, DB14/OS1, DB15/OS2.	58, 59, 60	DO/DI	Parallel Output/Input Data Bit 13, Data Bit 14, and Data Bit 15/Oversampling Rate Select. When SER / $\overline{PAR}$ = 0, these pins act as three-state parallel digital inputs/outputs. See the *Parallel Interface* section for details. In serial hardware mode, these pins control the oversampling settings. When full reset is released, the signal state is latched and requires another full reset to reconfigure. See the *Digital Filter* section for details. In software serial mode, these pins must be connected to DGND.
$\overline{WR}$ /BURST	61	DI	Write/burst mode enable. In software parallel mode, this pin is used as a parallel interface $\overline{WR}$. In hardware parallel or serial mode, this pin enables BURST mode. When full reset is released, the signal state is latched and requires another full reset to reconfigure. See *Burst Sequencer* section for details. In software serial mode, this pin should be connected to DGND.
SCLK/$\overline{RD}$	62	DI	Serial Clock Input/Parallel Data Read Control Input. In serial mode, this pin acts as the serial clock input for data transfer. The falling edge of $\overline{CS}$ takes the data output lines SDOA and SDOB out of three-state and outputs the MSB of the conversion result. The SCLK rising edge

PINS		PIN TYPE[1]	FUNCTION
NAME[2]	NUM		
			clocks all subsequent data bits into the serial data outputs SDOA and SDOB. In parallel mode, if both $\overline{CS}$ and RD are at logic low, the output bus is enabled.
$\overline{CS}$	63	DI	Chip Select. This active low logic input enables data frame transmission. In parallel mode, if both $\overline{CS}$ and RD are at logic low, the DBx output bus is enabled and the conversion results are output on the parallel data bus. In serial mode, $\overline{CS}$ frames the serial read transfer and clocks out the MSB of the serial output data.
CHSEL0, CHSEL1, CHSEL2.	64, 65, 66	DI	Channel Select Input 0 to Input 2. In hardware mode, these inputs select the input channels for the next conversion in Channel Group A and Channel Group B. For example, CHSELx = 0x000 selects V0A and V0B for the next conversion; CHSELx = 0x001 selects V1A and V1B for the next conversion. In software mode, these pins must be connected to DGND.
BUSY	67	DO	Busy Output. After the rising edge of CONVST, this pin goes to logic high, indicating that the conversion process has started. The BUSY output remains high until the conversion process of the currently selected channel is complete. The falling edge of BUSY indicates that the conversion data is being latched into the output data register and will be available for reading later. The data must be read after BUSY goes low. The rising edge of CONVST has no effect when the BUSY signal is high.
CONVST	68	DI	Conversion start input for channel group A and channel group B. This logic input starts conversions on the analog input channels. For the selected analog input pair, a conversion starts when CONVST goes from low to high. When burst mode and oversampling mode are disabled, a pair of channels is converted each time CONVST goes from low to high. In sequencer mode, when burst mode or oversampling mode is enabled, to perform the required number of conversions, CONVST only needs to go from low to high once.
REGGND	69	CAP	Internal analog regulator ground. This pin must be connected to the AGND plane of the system.
REGCAP	70	CAP	Decoupling capacitor pin for the internal analog regulator voltage output. This output pin should be independently decoupled to REGGND with a 10μF capacitor. The voltage at this pin is typically 1.87V.
V0B	73	AI	Channel 0 Analog Input, ADC B.
V0BGND	74	AI GND	Analog input ground pin. This pin corresponds to the analog input pin

PINS		PIN TYPE[1]	FUNCTION
NAME[2]	NUM		
			V0B.
V1B	75	AI	Channel 1 Analog Input, ADC B.
V1BGND	76	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V1B.
V2B	77	AI	Channel 2 Analog Input, ADC B.
V2BGND	78	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V2B.
V3B	79	AI	Channel 3 Analog Input, ADC B.
V3BGND	80	AI GND	Analog input ground pin. This pin corresponds to the analog input pin V3B.

1. AI = Analog Input, GND = Ground, P = Power, REF = Reference Voltage Input/Output, DI = Digital Input, DO = Digital Output, and CAP = Decoupling Capacitor Pin.
2. Note that throughout this data sheet, multifunction pins, such as SER/PAR, are referred to by either the entire pin name or a single function of the pin; for example, SER means only that function is relevant.

5 Parameter Information

5.1 Absolute Maximum Ratings

Unless otherwise stated, T_A = 25 °C.

PARAMETER	RATING
V_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to V_{CC} + 0.3 V
Analog input voltage to AGND[1]	±25 V
Digital input voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital output voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFINOUT to AGND	−0.3 V to V_{CC} + 0.3 V
Input current to any pin other than the power supply[1]	±10 mA
Operating temperature range	−40 °C to +125 °C
Storage temperature range	−65 °C to +150 °C
Junction temperature	150 °C
Reflow	
Lead-tin soldering temperature (10 seconds to 30 seconds)	240 (+0) °C
Lead-free soldering temperature	260 (+0) °C
ESD	
All pins except analog input	2 kV
Analog input pins only	7 kV

1. Transient currents below 100 mA will not cause silicon controlled rectifier (SCR) latch-up.
2. Caution: Stresses equal to or exceeding the absolute maximum ratings listed above may cause permanent damage to the product. These are maximum ratings only and do not imply that the device will operate normally under these conditions or any other conditions beyond those shown in the operational section of this technical specification. Long-term operation beyond the maximum rating conditions may affect product reliability.

5.2 Thermal Resistance

Thermal performance is directly related to the printed circuit board (PCB) design and the operating environment, and PCB heat dissipation design must be taken seriously. Θ_{JA} is the junction-to-ambient thermal resistance under natural convection, measured in a 1-cubic-foot sealed enclosure, and Θ_{JC} is the junction-to-case thermal resistance.

PACKAGE	Θ_{JA}	Θ_{JC}	UNIT
LQFP80[1]	41	7.5	°C/W

1. Thermal resistance simulation values are based on the JEDEC 2S2P thermal test board, see JEDEC JESD51.

5.3 Technical Specifications

Unless otherwise noted, V_{REF} = 2.5 V external/internal reference, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, f_{SAMPLE} = 1 MSPS, T_A = −40 °C to +125 °C.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Dynamic Performance	f_{IN} = 1 kHz sine wave				
Signal-to-Noise Ratio (SNR)[1]	No oversampling, ±10V range	89	90.5		dB
	No oversampling, ±5V range	87	88		
	No oversampling, ±2.5V range	85	86		
Signal-to-Noise/Distortion Ratio (SINAD)	No oversampling, ±10V range	88.5	90		dB
	No oversampling, ±5V range	86	87.5		
	No oversampling, ±2.5V range	84	85.5		
Dynamic Range	No oversampling, ±10V range		92		dB
	No oversampling, ±5V range		90.5		
	No oversampling, ±2.5V range		88		
Total Harmonic Distortion (THD)	No oversampling, ±10V range		−102	−93.5	dB
	No oversampling, ±5V range		−103		
	No oversampling, ±2.5V range		−104		
Peak harmonics or spurious noise			−102		dB
Channel-to-channel isolation	f_{IN} up to 5kHz for unselected channels		−106		dB
Analog Input Filter					
Full Power Bandwidth	−3 dB		25		kHz
	−0.1 dB		3.9		
Phase Delay[2]	±10 V range		6.9		µs
	±5V range		6.7		
	±2.5 V range		6		
Phase Delay Matching				200	ns
DC Accuracy					
Resolution	No missing codes	16			Bits
Differential Nonlinearity (DNL)			±0.5	±0.99	LSB[4]
Integral Nonlinearity (INL)			±1	±2	LSB
Total Unadjusted Error (TUE)	±10 V range		±6		LSB
	±5V range		±8		
	±2.5V range		±10		
Positive full scale error[4]					
External reference voltage source	±10V range		±3	±32	LSB
	±5V range		±4		
	±2.5V range		±5		
Internal voltage reference	±10V range		±3		LSB

Technical Specifications (Continued)

Unless otherwise noted, V_{REF} = 2.5 V external/internal reference, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, f_{SAMPLE} = 1 MSPS, T_A = −40 °C to +125 °C.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Positive Full Scale (PFS) Error Drift[2]	External reference voltage source		±2	±5	ppm/°C
	Internal voltage reference		±3	±10	
Positive Full-Scale Error Matching	±10V range		4		LSB
	±5V range		4		
	±2.5V range		8		
Bipolar Zero Code Error	±10V range		±1	±8	LSB
	±5V range		±1	±10	
	±2.5V range		±1.5	±15	
Bipolar Zero Code Error Drift [2]	±10V range		±6	±20.4	µV/°C
	±5V range		±3.6		
	±2.5V range		±2.5		
Bipolar Zero Code Error Matching	±10V range		±2	±10	LSB
	±5V range		±3		
	±2.5V range		±3		
Negative Full Scale (NFS) Error[4]	External reference voltage source				
	±10V range		±3	±32	LSB
	±5V range		±4		
	±2.5V range		±5		
	Internal voltage reference				
	±10V range		±3		LSB
Negative full scale error drift[2]	External reference voltage source		±2	±5	ppm/°C
	Internal voltage reference		±3	10	
Negative Full Scale Error Matching	±10V range		4		LSB
	±5V range		4		
	±2.5V range		8		
Analog Input					
Input voltage range	Software/Hardware Optional			±10	V
	Software/Hardware Optional			±5	
	Software/Hardware Optional			±2.5	
Analog input current	±10V range		10		µA
	±5V range		5		µA
	±2.5V range		2.5		µA
Input Capacitor[5]			5		pF
Input Impedance	See *Analog Input* section	1			MΩ

Technical Specifications (Continued)

Unless otherwise noted, V_{REF} = 2.5 V external/internal reference, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, f_{SAMPLE} = 1 MSPS, T_A = −40 °C to +125 °C.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Reference voltage input/output					
Reference input voltage range	See the *ADC Transfer Function* section	2.495	2.5	2.505	V
DC leakage current				±0.1	µA
Input Capacitor[5]	REFSEL = 1		7.5		pF
Reference output voltage	REFINOUT	2.495	2.5	2.505	V
Reference source temperature coefficient [2]			±3	±15	ppm/°C
Logic Input					
Input voltage					
High (V_{INH})	V_{DRIVE} = 2.7 V to 3.6 V	2			V
	V_{DRIVE} = 2.3 V to 2.7 V	1.7			
Low (V_{INL})	V_{DRIVE} = 2.7 V to 3.6 V			0.8	V
	V_{DRIVE} = 2.3 V to 2.7 V			0.7	
Input Current (I_{IN})				±1	µA
Input Capacitor (C_{IN})[5]			5		pF
Logic Output					
Output voltage					
High (V_{OH})	I_{SOURCE} = 100 µA	V_{DRIVE} − 0.2			V
Low (V_{OL})	I_{SINK} = 100 µA			0.4	V
Floating state leakage current			±0.005	±1	µA
Floating output capacitance[5]			5		pF
Output Encoding	Two's complement				
Conversion Rate					
Conversion time	Each pair of channels		0.55		µs
Collection time	Each pair of channels		0.45		µs
Throughput rate	Each pair of channels			1	MSPS
Power Requirements					
V_{CC}		4.75		5.25	V
V_{DRIVE}		2.3		3.6	V
I_{VCC}					
Normal Mode					
Static			21	27	mA
Operational	f_{SAMPLE} = 1MSPS		25	31	mA
Shutdown Mode			4		µA

Technical Specifications (Continued)

Unless otherwise noted, V_{REF} = 2.5 V external/internal reference, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, f_{SAMPLE} = 1 MSPS, T_A = −40 °C to +125 °C.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
I_{DRIVE}	Digital input = 0V or V_{DRIVE}				
Normal Mode					
Static			0.7	0.85	mA
Operation	f_{SAMPLE} = 1MSPS		4.6	4.9	mA
Shutdown Mode			85		μA
Power consumption					
Normal Mode					
Static			130	150	mW
Operation	f_{SAMPLE} = 1MSPS		160	180	mW
Shutdown Mode			2.8		mW

1. By enabling oversampling, the user can achieve 93 dB SNR, these values are valid for manual mode, in burst mode these values are reduced by approximately 1 dB.
2. Not production tested. Samples are tested during initial release to ensure compliance with standards.
3. LSB stands for least significant bit. For ±2.5 V input range, 1LSB = 76.293 μV; for ±5 V input range, 1LSB = 152.58 μV; for ±10 V input range, 1LSB = 305.175 μV.
4. The positive and negative full-scale errors of the internal reference do not include the reference error.
5. Simulation data support.

5.4 General Timing Specifications

V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, V_{REF} = 2.5 V external/internal reference, T_A = −40 °C to +125 °C, unless otherwise noted. Interface timing is tested with 30pF load capacitance and is dependent on V_{DRIVE} and the load capacitance of the serial interface.

PARAMETER[1]	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYCLE}	Minimum time between consecutive CONVST rising edges (excluding burst and oversampling modes)	1			µs
t_{CONV_LOW}	CONVST low level pulse width	80			ns
t_{CONV_HIGH}	CONVST high level pulse width	80			ns
t_{BUSY_DELAY}	CONVST high to BUSY high (manual mode)			32	ns
t_{CS_SETUP}	BUSY falling edge to $\overline{CS}$ falling edge setup time	20			ns
t_{CH_SETUP}	Channel selection setup time for CHSELx in hardware mode	50			ns
t_{CH_HOLD}	Channel selection hold time of CHSELx in hardware mode	20			ns
t_{CONV}	Conversion time for selected channel pair		475	520	ns
t_{ACQ}	Acquisition time for the selected channel pair	480			ns
t_{QUIET}	$\overline{CS}$ rising edge to the next CONVST rising edge	50			ns
$t_{\overline{RESET}\_LOW}$					
Partial Reset	Partial $\overline{RESET}$ low level pulse width	40		500	ns
Complete reset	Full $\overline{RESET}$ low level pulse width	1.2			µs
t_{DEVICE_SETUP}					
Partial Reset	The time between the high level of the part CONVST and the rising edge of $\overline{RESET}$	50			ns
Complete reset	The time between the full high level of CONVST and the rising edge of $\overline{RESET}$	15			ms
t_{WRITE}					
Partial Reset	For write operations, $\overline{RESET}$ the time between the high level and $\overline{CS}$	50			ns
Complete reset	For write operations, $\overline{RESET}$ the time between fully high and $\overline{CS}$	240			µs
$t_{\overline{RESET}\_WAIT}$	Time between stabilizing VCC/VDRIVE and releasing $\overline{RESET}$	1			ms
$t_{\overline{RESET}\_SETUP}$	$\overline{RESET}$ The time that the queried hardware input must remain stable before being released				
Partial Reset		10			ns
Complete reset		0.05			ms
$t_{\overline{RESET}\_HOLD}$	$\overline{RESET}$ The time after release that the queried hardware input must remain stable				
Partial Reset		10			ns
Complete reset		0.24			ms

1. Not production tested. Samples are tested during initial release to ensure compliance with standards.

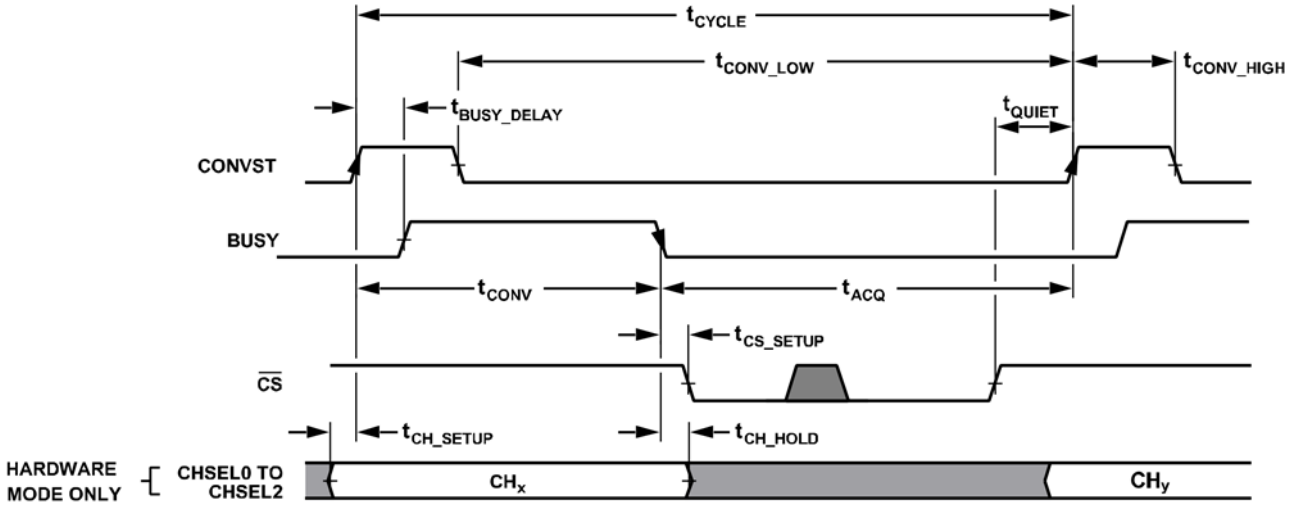


Figure 2. Universal Timing Diagram Across All Interfaces

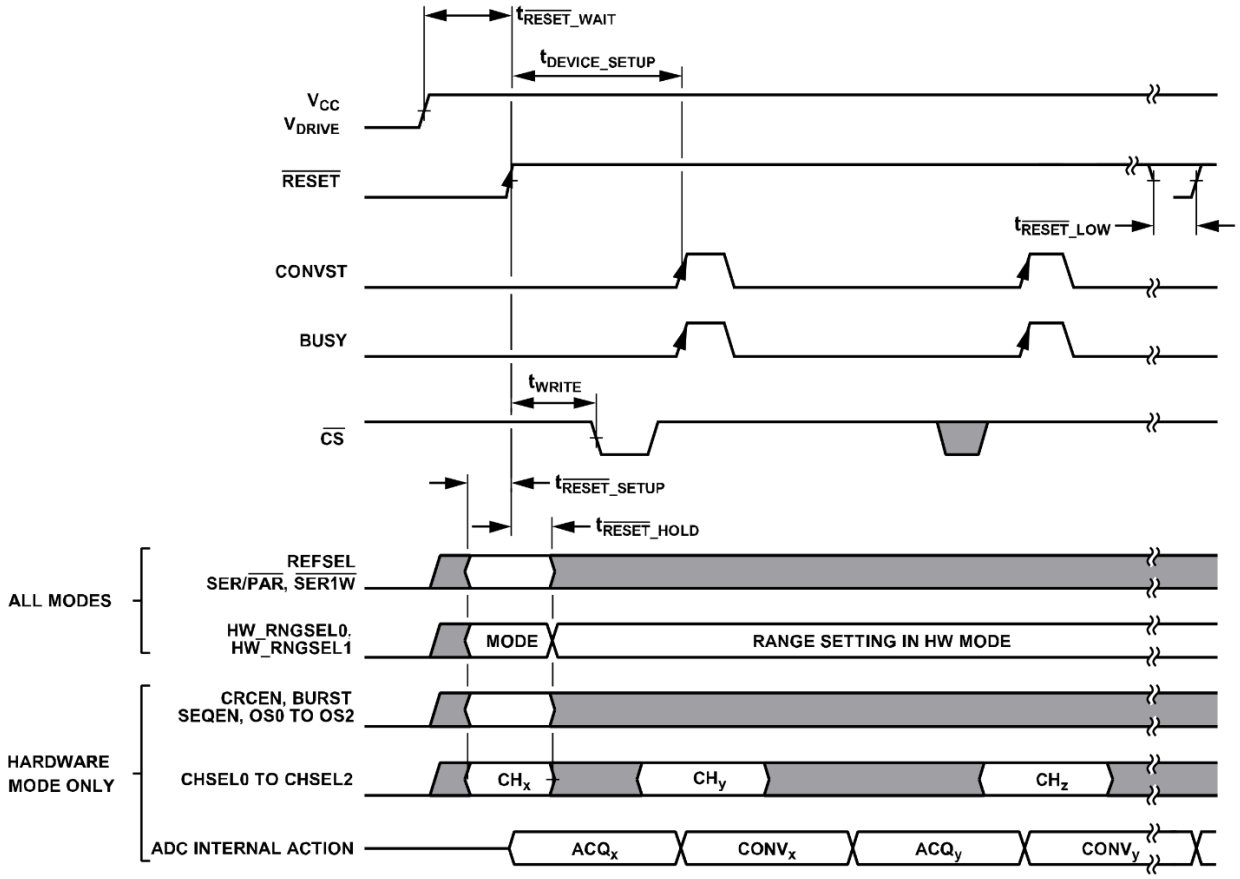


Figure 3. Reset Timing Diagram

5.5 Parallel Mode Timing Specifications

PARAMETER	MIN	TYP	MAZ	UNIT	DESCRIPTION
t_{RD_SETUP}	0			ns	$\overline{CS}$ falling edge to $\overline{RD}$ falling edge setup time
t_{RD_HOLD}	0			ns	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge hold time
t_{RD_HIGH}	10			ns	$\overline{RD}$ high level pulse time
t_{RD_LOW}	30			ns	$\overline{RD}$ low level pulse time
t_{DOUT_SETUP}			30	ns	Data access time after the falling edge $\overline{RD}$
t_{DOUT_3STATE}			11	ns	$\overline{CS}$ rising edge to DBx high impedance state
t_{WR_SETUP}	10			ns	$\overline{CS}$ to $\overline{WR}$ set-up time
t_{WR_HIGH}	20			ns	$\overline{WR}$ high level pulse time
t_{WR_LOW}	30			ns	$\overline{WR}$ low level pulse time
t_{WR_HOLD}	10			ns	$\overline{WR}$ hold time
t_{DIN_SETUP}	30			ns	Configuration data to $\overline{WR}$ set-up time
t_{DIN_HOLD}	10			ns	Configuration data to $\overline{WR}$ hold time
t_{CONF_SETTLE}	20			ns	Configuration data stabilization time，$\overline{WR}$ rising edge to CONVST rising edge

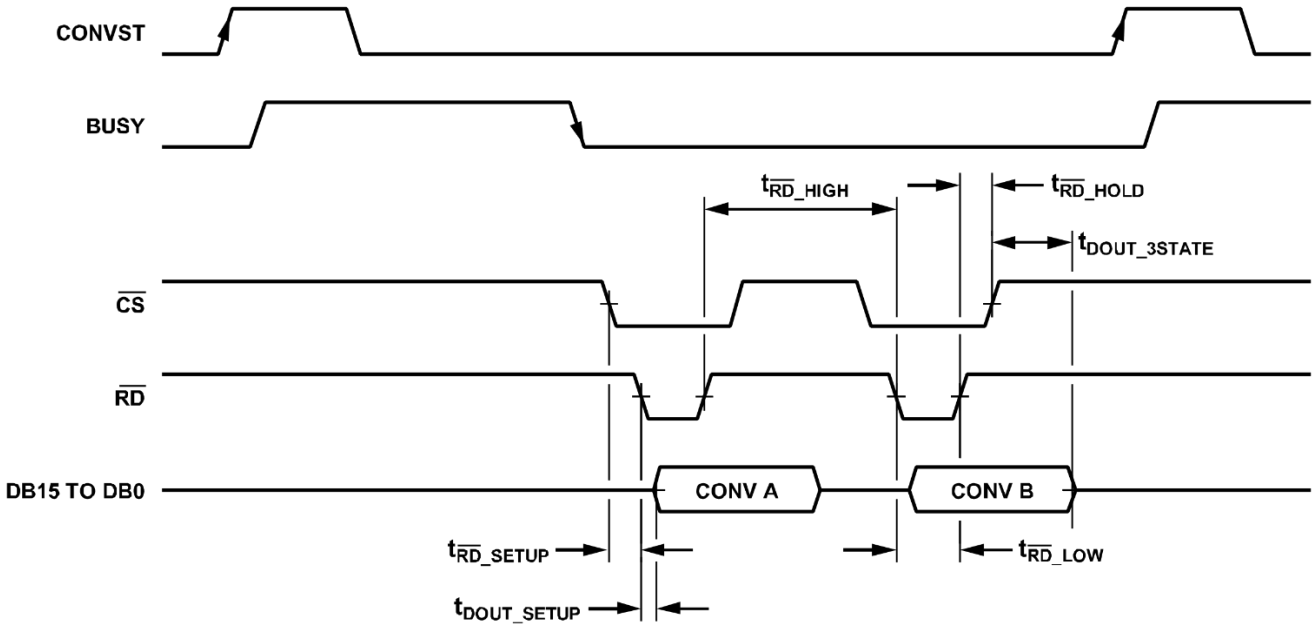


Figure 4. Parallel Read Timing Diagram

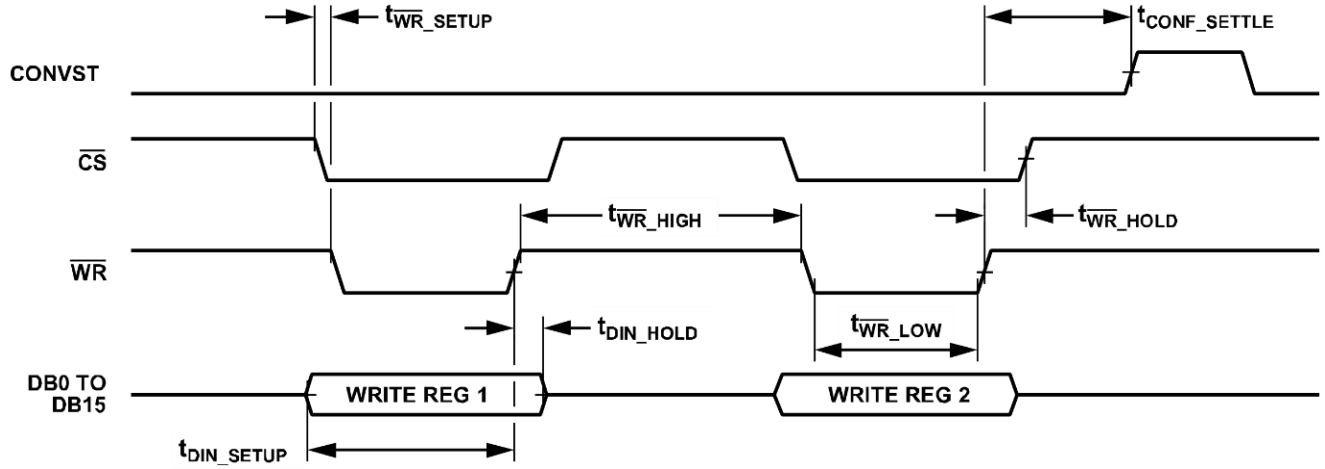


Figure 5. Parallel Write Timing Diagram

5.6 Serial Mode Timing Specifications

PARAMETER	MIN	TYP	MAZ	UNIT	DESCRIPTION
f_{SCLK}[1]			40/50	MHz	SCLK Frequency
t_{SCLK}	1/f_{SCLK}				Minimum SCLK period
t_{SCLK_SETUP}[1]	10.5			ns	$\overline{CS}$ to SCLK falling edge set-up time，V_{DRIVE} higher than 3V
	13.5			ns	$\overline{CS}$ to SCLK falling edge set-up time，V_{DRIVE} higher than 2.3V
t_{SCLK_HOLD}	10			ns	SCLK to $\overline{CS}$ rising edge hold time
t_{SCLK_LOW}	8			ns	SCLK low-level pulse width
t_{SCLK_HIGH}	9			ns	SCLK high-level pulse width
t_{DOUT_SETUP}[1]			9	ns	SCLK data output access time after the rising edge，V_{DRIVE} higher than 3 V
			11	ns	SCLK data output access time after the rising edge，V_{DRIVE} higher than 2.3 V
t_{DOUT_HOLD}	4			ns	SCLK data output access time after the rising edge
t_{DIN_SETUP}	10			ns	SCLK data input setup time before the falling edge
t_{DIN_HOLD}	8			ns	SCLK data input hold time after the falling edge
t_{DOUT_3STATE}			10	ns	$\overline{CS}$ rising edge to SDOx high impedance

1. Depends on VDRIVE and the load capacitance (see Table 6).

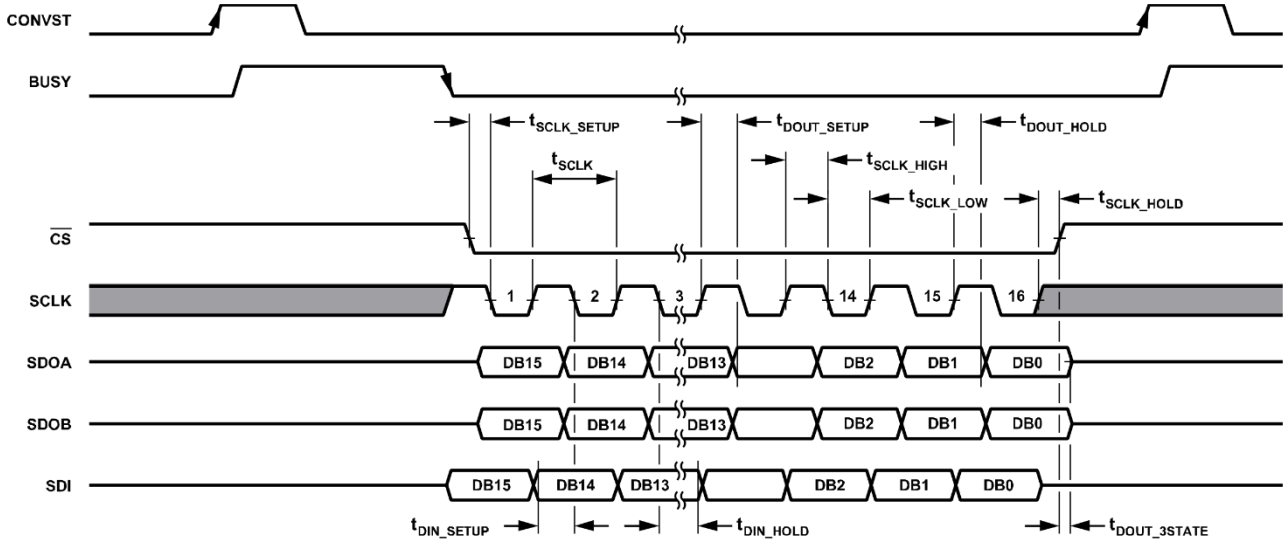


Figure 6. Serial Timing Diagram

5.7 Typical Performance Characteristics

Unless otherwise noted, V_{REF} = 2.5 V (internal), V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, T_A = 25 °C.

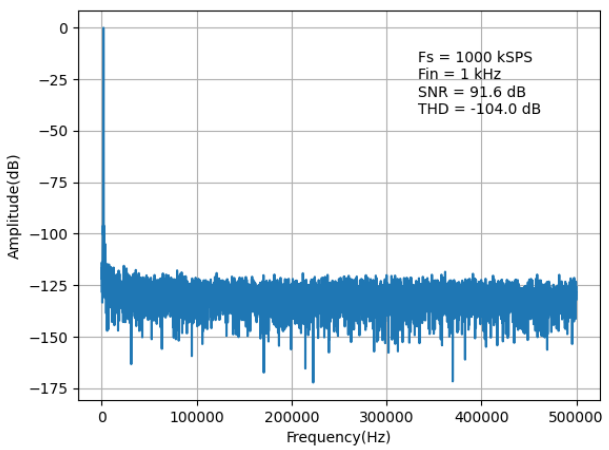


Figure 7. Fast Fourier Transform (FFT), ±10V Range

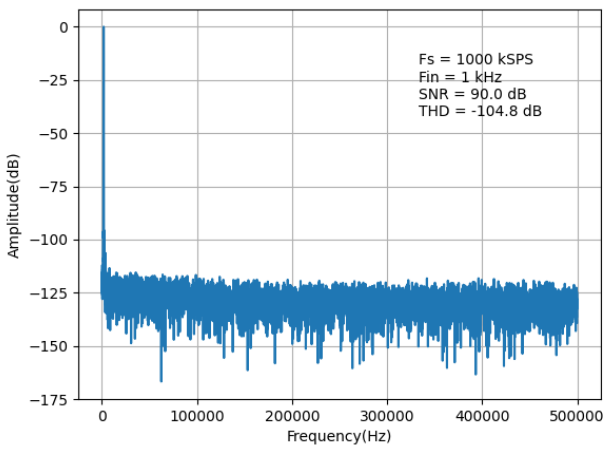


Figure 8. Fast Fourier Transform (FFT), ±5V Range

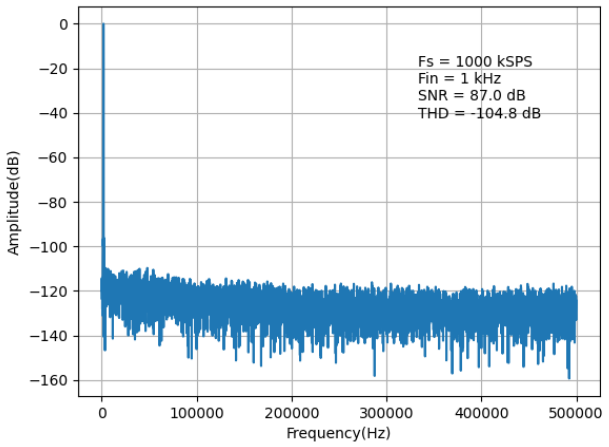


Figure 9. Fast Fourier Transform (FFT), ±2.5V Range

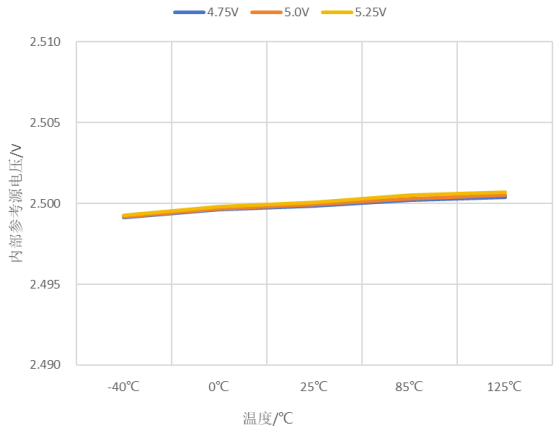


Figure 10. Internal Reference Source Temperature Characteristics

Typical Performance Characteristics (Continued)

Unless otherwise noted, V_{REF} = 2.5 V (internal), V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, T_A = 25 °C.

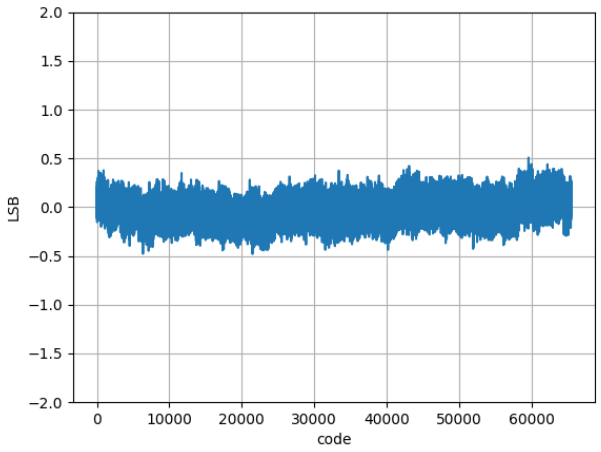


Figure 11. Typical INL, ±10V Range

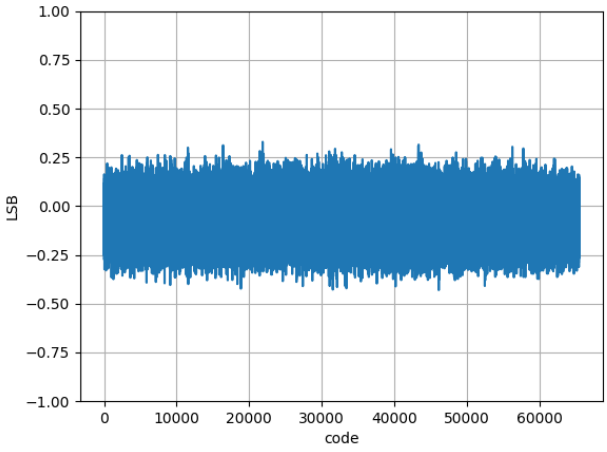


Figure 12. Typical DNL, ±10V Range

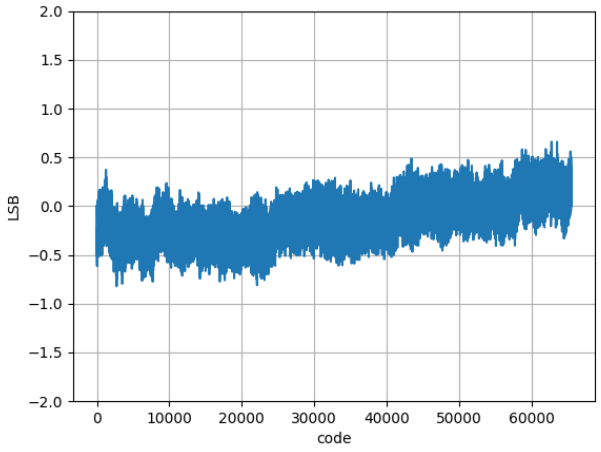


Figure 13. Typical INL, ±5V Range

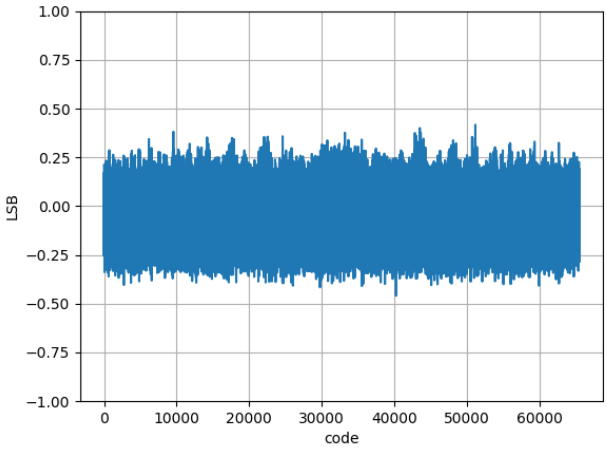


Figure 14. Typical DNL, ±5V Range

Typical Performance Characteristics (Continued)

Unless otherwise noted, V_{REF} = 2.5 V (internal), V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, T_A = 25 °C.

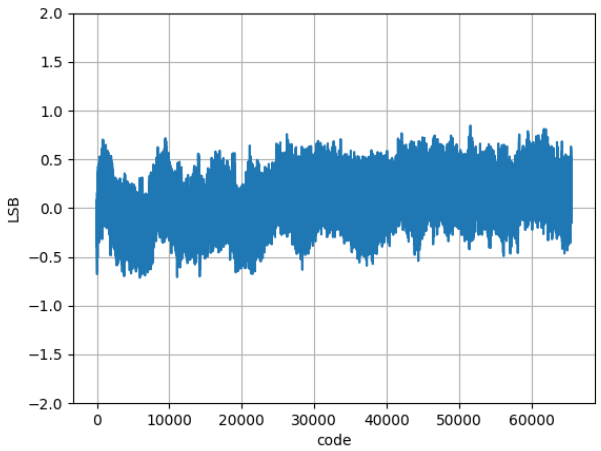


Figure 15. Typical INL, ±2.5V Range

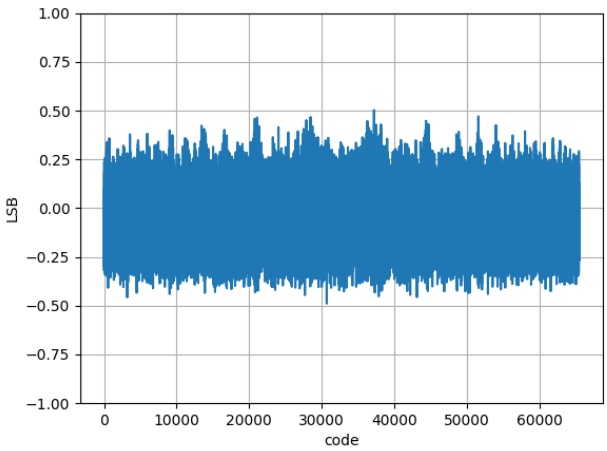


Figure 16. Typical DNL, ±2.5V Range

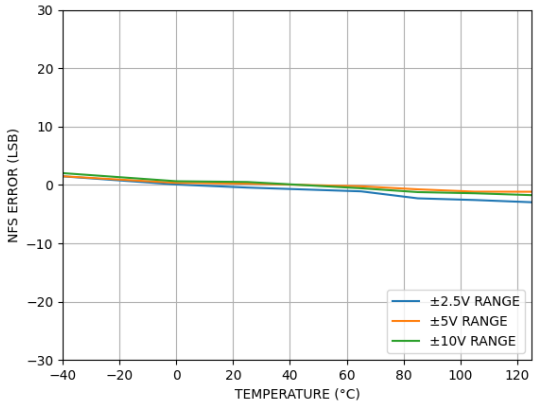


Figure 17. PFS Error vs Temperature

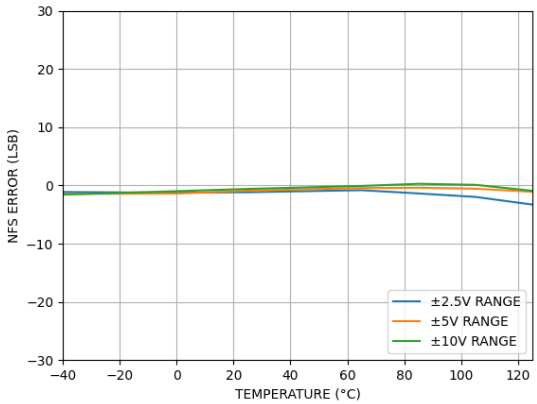


Figure 18. NFS Error vs Temperature

Typical Performance Characteristics (Continued)

Unless otherwise noted, V_{REF} = 2.5 V (internal), V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, T_A = 25 °C.

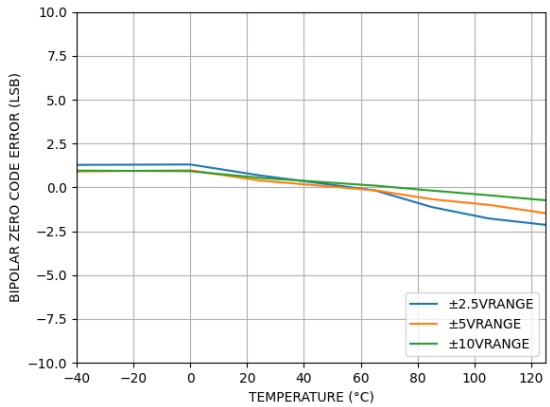


Figure 19. Bipolar Zero Code Error vs Temperature

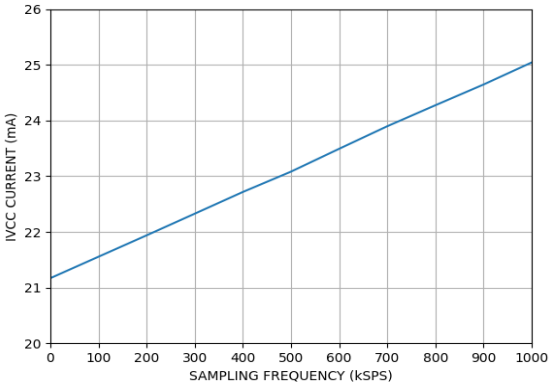


Figure 20. IVCC vs Sampling Rate

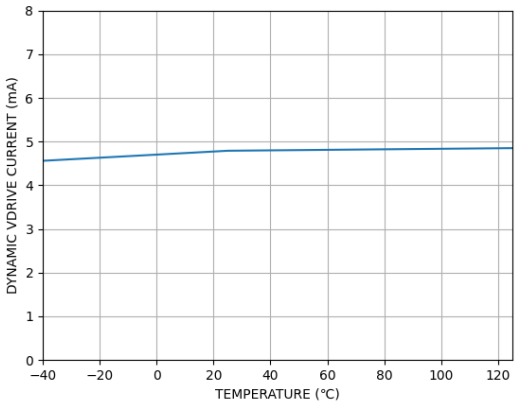


Figure 21. Dynamic VDRIVE vsTemperature

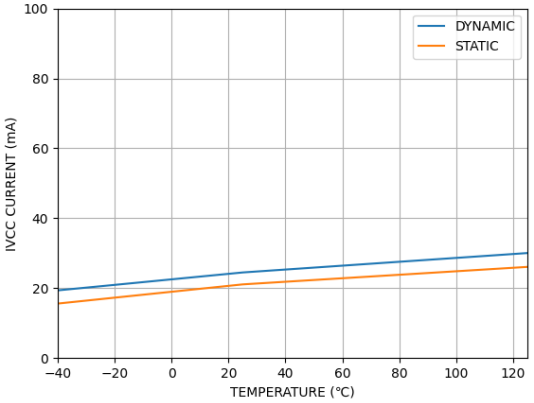


Figure 22. IVCC vs Temperature

Typical Performance Characteristics (Continued)

Unless otherwise noted, V_{REF} = 2.5 V (internal), V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, T_A = 25 °C.

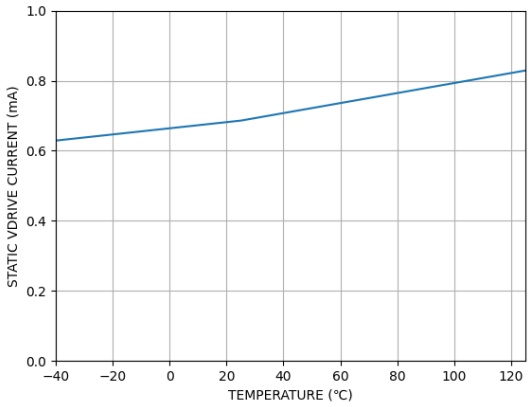


Figure 23. Static VDRIVE vs Temperature

6 Functional Description

6.1 Converter Details

The GD30AD33G0 is a data acquisition system that uses a high-speed, low-power, charge redistribution successive approximation analog-to-digital converter (ADC) that can perform dual-channel simultaneous sampling of 16 analog input channels. The analog inputs of the GD30AD33G0 can accept true bipolar input signals. The analog input range options are ±10 V, ±5 V, and ±2.5 V. The GD30AD33G0 is powered by a single 5 V power supply.

The GD30AD33G0 has built-in input clamp protection, input signal scaling amplifier, first-order anti-aliasing filter, on-chip reference voltage source, reference voltage buffer, dual high-speed ADC, digital filter, flexible sequencer, and high-speed parallel and serial interfaces.

By controlling the HW_RNGSELx pins, the GD30AD33G0 can work in hardware or software mode. In hardware mode, the GD30AD33G0 is configured by pin control. In software mode, the GD30AD33G0 is configured by control registers (accessed through serial or parallel interfaces).

6.2 Analog Input

6.2.1 Analog Input Channel Selection

GD30AD33G0 has built-in dual synchronous sampling 16-bit ADC. Each ADC has 8 analog input channels, for a total of 16 analog inputs. In addition, GD30AD33G0 has an on-chip diagnostic channel for monitoring the VCC power supply, as well as an on-chip adjustable low-dropout regulator. Channels can be selected for conversion by controlling the CHSELx pin in hardware mode or by controlling the channel register in software mode. To sample the diagnostic channel, software mode must be used. GD30AD33G0 can dynamically select channels or pre-set the channels to be converted using the on-chip sequencer. In hardware mode, only the corresponding A and B channels can be sampled synchronously, that is, channel V0A is always sampled together with channel V0B. In software mode, any A channel can be selected for synchronous sampling with any B channel.

6.2.2 Analog Input Range

The GD30AD33G0 can handle true bipolar and single-ended input voltages. The logic level of the range selection pins HW_RNGSEL0 and HW_RNGSEL1 determines the analog input range of all analog input channels. If both range selection pins are connected to logic low, the analog input range in software mode is determined by the input range register (see the " *Register Summary*" section for details). In software mode, a separate analog input range can be configured for each channel.

Table 1. Analog Input Range Selection

Analog Input Range	HW_RNGSEL1	HW_RNGSEL0
Configured by input range register	0	0
±2.5 V	0	1
±5 V	1	0
10 V	1	1

In hardware mode, a change in the logic state of these pins affects the analog input range immediately, however, there is a typical settling time requirement of approximately 120 µs in addition to the normal acquisition time requirement. It is recommended that the range select pins be hardwired based on the input range required by the system signal.

6.2.3 Analog Input Impedance

The analog input impedance of GD30AD33G0 is 1 MΩ, which is a fixed input impedance that does not change with the sampling frequency of GD30AD33G0. The high analog input impedance can eliminate the driver amplifier at the front end of GD30AD33G0, allowing it to be directly connected to the signal source or sensor.

6.2.4 Analog Input Clamp Protection

The figure below shows the analog input circuit of the GD30AD33G0. Each analog input of the GD30AD33G0 contains a clamp protection circuit. Although it is powered by a single 5 V supply, this analog input clamp protection allows input overvoltages from −25 V to +25 V.

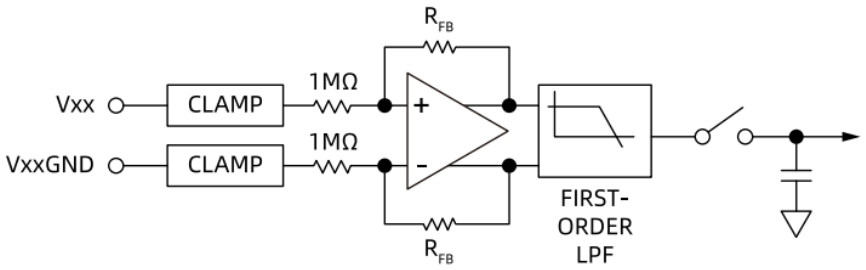


Figure 24. Analog Input Circuit

The following figure shows the input clamp current vs. source voltage characteristics of the clamp circuit. For source voltages from −20 V to +20 V, there is no current in the clamp circuit. When the input voltage is above +25 V or below −25 V, the GD30AD33G0 clamp circuit turns on.

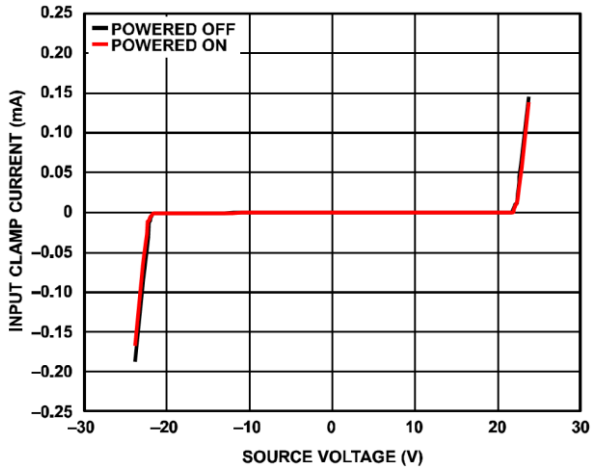


Figure 25. Input Protection Clamp Curve, Input Clamp Current vs. Source Voltage

A series resistor should be placed on the analog input channel to limit the current to less than ±10 mA when the input voltage is above +20 V or below −20 V. If there is a series resistor on the analog input channel VxA or VxB,

a corresponding resistor is also required on the analog input ground channel VxAGND or VxBGND (see the figure below). If there is no corresponding resistor on the VxAGND or VxBGND channel, the channel will have an offset error. An input overvoltage clamp protection circuit should be used to protect the GD30AD33G0 from transient overvoltage events. It is recommended not to place the GD30AD33G0 in a condition where the clamp protection circuit is active for a long time (normal or power-down condition).

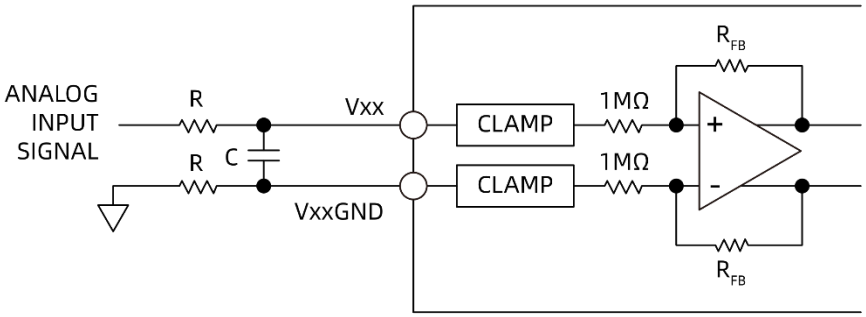


Figure 26. Input Resistance Matching of Analog Inputs

6.2.5 Analog Input Anti-Aliasing Filter

The GD30AD33G0 also provides an analog anti-aliasing filter (first-order Butterworth filter). The following figures show the frequency and phase responses of the analog anti-aliasing filter, respectively. The typical corner frequency is 39 kHz for the ±10 V range and 33 kHz for the ±5 V range.

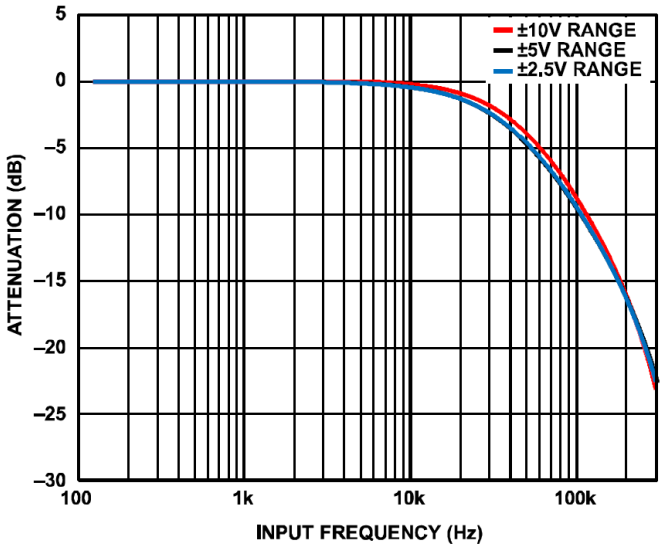


Figure 27. Simulated Anti-Aliasing Filter Drequency Response

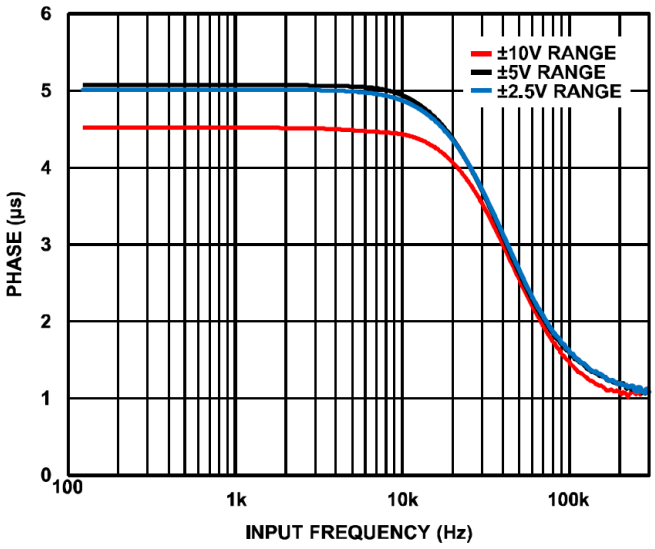
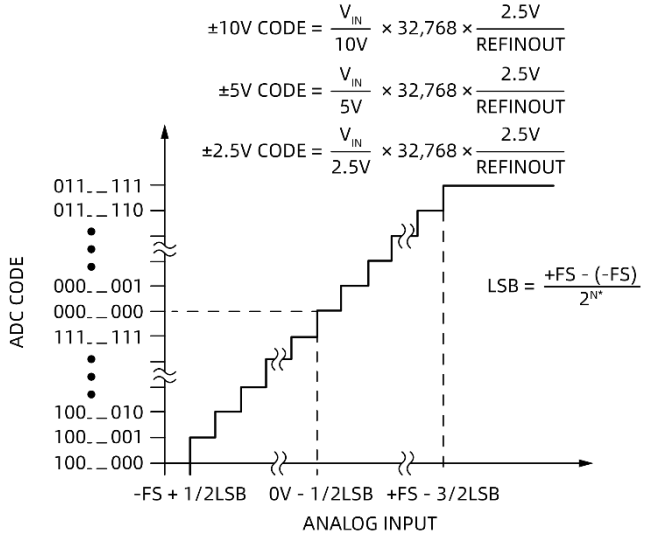


Figure 28. Simulated Anti-Aliasing Filter Phase Response

6.3 ADC Transfer Function

The output encoding of the GD30AD33G0 is two's complement. The designed code transition is performed in the middle of consecutive LSB integer values (i.e., 1/2 LSB and 3/2 LSB). For the GD30AD33G0, the LSB size is the full-scale range divided by 65,536. The ideal transfer characteristic of the GD30AD33G0 is shown in the figure below. The LSB size depends on the selected analog input range.



	+FS	MIDSCALE	-FS	LSB
±10V RANGE	+10V	0V	-10V	305µV
±5V RANGE	+5V	0V	-5V	152µV
±2.5V RANGE	+2.5V	0V	-2.5V	76µV

*WHERE N IS THE NUMBER OF BITS OF THE CONVERTER

Figure 29. Transfer Characteristics

6.4 Internal/External Reference Voltage Source

The GD30AD33G0 can operate with either an internal or external reference voltage source, and it has an internal 2.5 V bandgap reference voltage source. The REFINOUT pin can use this 2.5 V reference voltage to generate the 4.096 V internal reference voltage, or it can allow a 2.5 V external reference voltage to be applied to the GD30AD33G0. The applied 2.5 V external reference voltage is also amplified to 4.096 V by the internal buffer. This 4.096 V buffered reference voltage is the reference voltage used by the SAR ADC.

The REFSEL pin is a logic input pin that allows the user to select an internal reference voltage or an external reference voltage. If this pin is set to a logic high, the internal reference voltage mode is selected and enabled. If this pin is set to a logic low, the internal reference voltage is disabled and an external reference voltage must be applied to the REFINOUT pin.

The internal reference buffer is always enabled. After a full reset, the GD30AD33G0 operates in the reference mode selected by the REFSEL pin. Whether using an internal or external reference, the REFINOUT pin needs to be decoupled. A 100 nF X8R ceramic capacitor needs to be connected from the REFINOUT pin to REFINOUTGND.

The GD30AD33G0 has a built-in reference voltage buffer that is configured to amplify the reference voltage to approximately 4.096 V. A 10 µF X5R ceramic capacitor needs to be connected between REFCAP and REFGND. The reference voltage provided by the REFINOUT pin is 2.5 V. When the GD30AD33G0 is configured in external reference voltage mode, the REFINOUT pin is a high input impedance pin.

If the internal reference voltage needs to be used elsewhere in the system, it must first be buffered externally.

6.5 Shutdown Mode

When the RESET pin remains low for more than 1.2 µs, the GD30AD33G0 enters shutdown mode. When the RESET pin changes from low to high, the device exits shutdown mode and enters normal mode.

When the GD30AD33G0 is in shutdown mode, the typical power consumption is 78 µA, and the time from power-on to writing to the device is about 240 µs. The time from power-on to conversion execution is 15 ms. In shutdown mode, all circuits are shut down and all registers are cleared and reset to their default values.

6.6 Digital Filter

The GD30AD33G0 has an optional digital first-order sinc filter built in, which must be used in applications that use lower throughput rates or require higher signal-to-noise ratios or wider dynamic range.

The OSR of the digital filter is controlled by the oversampling pins OS2 to OS0 (OSx) in hardware mode and by the OS bit in the configuration register in software mode. In software mode, oversampling is enabled for all channels after the OS bit in the configuration register is set. In hardware mode, the OSx signal at full reset release determines the OSR to be used.

If the OSx pin/OS bit selects 8x oversampling, the next CONVST rising edge acquires the first sample of the selected channel, and the remaining 7 samples of the channel are acquired by the internally generated sampling signal. These samples are then averaged to improve SNR performance. As the oversampling ratio increases, the −3dB bandwidth decreases and the allowed sampling frequency also decreases. The conversion time increases with the oversampling ratio, and the BUSY signal is proportional to the oversampling ratio. The acquisition and

conversion times increase linearly with the oversampling ratio.

If oversampling is enabled in sequencer or burst mode, an additional sample is acquired for a given channel before the sequencer moves to the next channel.

7 Application Information

7.1 Functional Block Diagram

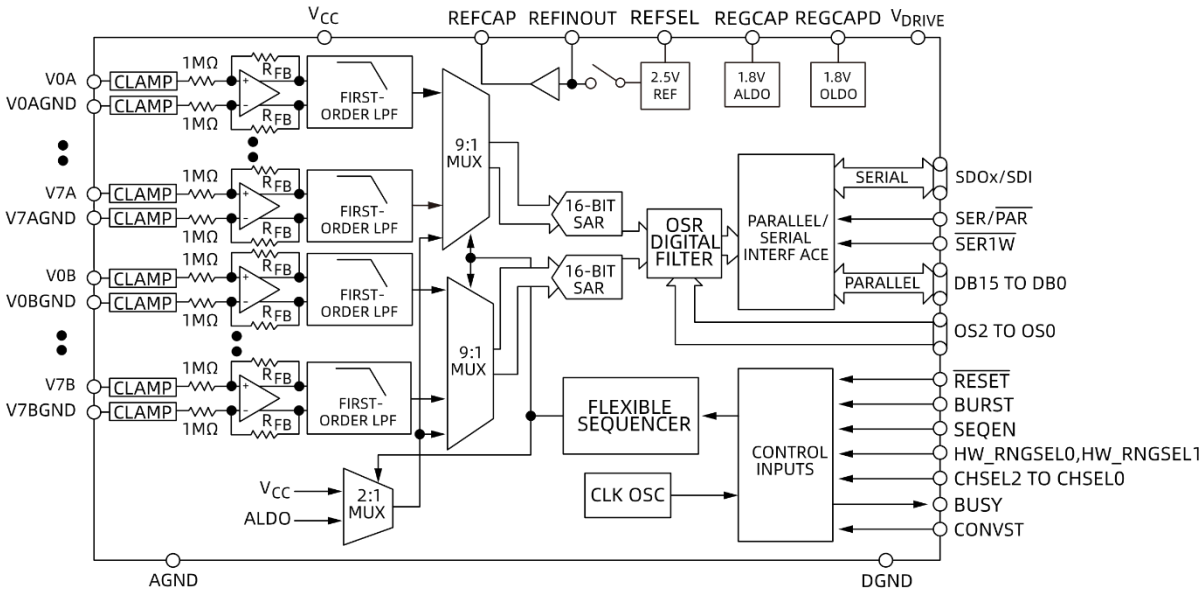


Figure 30. GD30AD33G0 Functional Block Diagram

7.2 Functional Overview

GD30AD33G0 has two main working modes: hardware mode and software mode. In addition, the communication interface of hardware or software mode can be serial or parallel. For different working modes and interface selections, some functions may not be available. In software serial mode and software parallel mode, all functions are available; in hardware serial mode and hardware parallel mode, some functions are restricted. Table 2 lists the functions that can be used in different working modes.

7.3 Power Supply

GD30AD33G0 has two independent power supplies V_{CC} and V_{DRIVE}, which are used to power analog circuits and digital interfaces respectively. Both V_{CC} and V_{DRIVE} should be decoupled through parallel 10 µF and 100 nF capacitors.

Additionally, these supplies are regulated by two internal LDO regulators. The analog LDO (ALDO) typically provides 1.9 V. ALDO should be decoupled with a 10 µF capacitor between the REGCAP and REGCAPGND pins. The digital LDO(DLDO) typically provides 1.85 V. DLDO should be decoupled with a 10 µF capacitor between the REGCAPD and REGCAPDGND pins.

7.4 Typical Connection

Figure 31 shows the typical connections required for proper operation of the GD30AD33G0. Decouple the V_{CC} and V_{DRIVE} supplies as shown in the figure below. Smaller 0.1 µF capacitors should be placed as close to the supply pins as possible with larger 10 µF bulk capacitors in parallel. Decouple the reference and LDO regulators as shown in the figure below and as described by the pin functions.

The analog input pins require matching resistors, R, at the VxA and VxAGND (similarly, VxB and VxBGND) inputs to avoid impedance mismatch causing gain errors on the analog input channels.

Table 2. Functional Matrix

Function	Working Mode[1]			
	Software mode, HW_RNGSELx=00		Hardware mode, HW_RNGSELx ≠ 00	
	Serial, SER/ PAR=1	Parallel, SER/ PAR=0	Serial, SER/ PAR=1	Parallel, SER/ PAR=0
Internal/external reference voltage source	Yes	Yes	Yes	Yes
Selectable analog input ranges				
Independent channel configuration	Yes	Yes	No	No
Unified channel configuration	No	No	Yes	Yes
Sequential Sequencer	Yes	Yes	Yes	Yes
Fully configurable sequencer	Yes	Yes	No	No
Burst Mode	Yes	Yes	Yes	Yes
On-chip oversampling	Yes	Yes	Yes	No
Diagnostic channel switching	Yes	Yes	No	No
Hardware Reset	Yes	Yes	Yes	Yes
Serial 1-wire mode	Yes	No	Yes	No
Serial 2-wire mode	Yes	No	Yes	No
Register Access	Yes	Yes	No	No

1. "Yes" means available, "No" means unavailable.

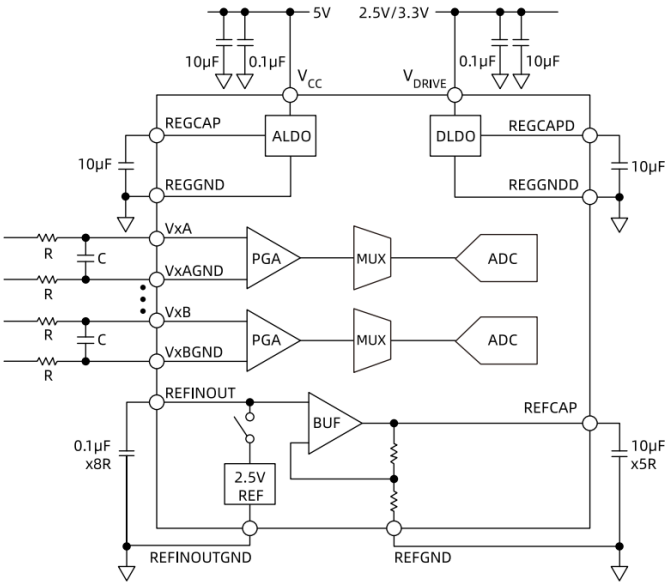


Figure 31. Typical External Connections

8 Device Configuration

8.1 Working Mode

The operating mode (hardware mode or software mode) is configured when the GD30AD33G0 exits full reset. The logic level of the HW_RNGSELx pin when the pin $\overline{\text{RESET}}$ changes from low to high determines the operating mode. The HW_RNGSELx pin has dual functions. If HW_RNGSELx = 0b00, the GD30AD33G0 enters software mode. Any other combination of HW_RNGSELx configures the GD30AD33G0 to hardware mode, and the analog input range configuration is shown in Table 1. After configuring software mode, the logic level of the HW_RNGSELx signal is ignored. After configuring an operating mode, to exit that operating mode and set another operating mode, a full reset is required through the $\overline{\text{RESET}}$ pins. If hardware mode is selected, all subsequent device configuration is performed through pin control. Access to on-chip registers is prohibited in hardware mode. In software mode, interface and reference voltage configuration must be performed through pin control, but all subsequent device configuration can only be performed through registers.

8.2 Internal/External Reference Voltage Source

When the GD30AD33G0 exits full reset, the internal reference is either enabled or disabled. The logic level of the REFSEL signal configures the reference when the pin $\overline{\text{RESET}}$ changes from low to high. Once the reference is configured, changes in the logic level of the REFSEL signal are ignored. If the REFSEL signal is set to 1, the internal reference is enabled. If REFSEL is set to logic 0, the internal reference is disabled and an external reference must be applied to the REFINOUT pin for the GD30AD33G0 to operate properly. A full reset through the pin $\overline{\text{RESET}}$ is required to exit the current operating mode and set another operating mode.

A 100 nF capacitor should be connected between the REFINOUT and REFINOUTGND pins. If an external reference voltage source is used, a 10 kΩ bandwidth limiting resistor should be connected in series between the reference voltage source and the REFINOUT pin of the GD30AD33G0.

8.3 Digital Interface

The digital interface selection (parallel or serial) is configured when the GD30AD33G0 exits full reset. When the $\overline{\text{RESET}}$ pin changes from low to high, the logic level of the $\text{SER}/\overline{\text{PAR}}$ signal configures the interface. If the $\text{SER}/\overline{\text{PAR}}$ signal is set to 0, the parallel interface is enabled. If the $\text{SER}/\overline{\text{PAR}}$ signal is set to 1, the serial interface is selected. In addition, if the serial interface is selected, when the $\overline{\text{RESET}}$ pin is released, the $\overline{\text{SER1W}}$ signal is monitored to determine whether serial 1-wire or 2-wire mode is selected. After the interface is configured, the $\text{SER}/\overline{\text{PAR}}$ signal or the logic level change of the $\overline{\text{SER1W}}$ signal (when the serial interface is enabled) is ignored. To exit the current operating mode and set another operating mode, a full reset is required through the $\overline{\text{RESET}}$ pin.

8.4 Hardware Mode

If hardware mode is selected, the available functions are limited and all functions are configured through pin control. To configure the functions of the GD30AD33G0, the logic levels of the following signals are checked after a full reset: BURST, SEQEN, and OSx. Table 3 summarizes the signals latched by the device when the full reset is released, depending on the selected operating mode. After completing the device configuration, to exit the current configuration and set another configuration, a full reset is required through the $\overline{\text{RESET}}$ pins. Depending

on the selected interface type, the available functions may be limited. For a complete list of available functions in hardware parallel or serial mode, see Table 2.

The CHSELx pin state is polled at reset to determine which initial analog input channel pair to acquire for conversion or to configure the initial settings of the sequencer. The channel pair to be converted or the hardware sequencer can be reconfigured during normal operation by setting and holding the CHSELx signal level before the rising edge of CONVST and until the falling edge of BUSY.

The HW_RNGSELx signals control the analog input range for all 16 analog input channels. Changes in the logic state of these pins immediately affect the analog input range; however, there is a typical settling time requirement of approximately 120 μs in addition to the normal acquisition time requirement. It is recommended that the range select pins be hardwired based on the input range required by the system signal.

Access to on-chip registers is prohibited in hardware mode.

Table 3. Latch Hardware Summary

Signal	Latched when fully reset		Read at reset		Busy time reading		Edge Drive	
	Hardware Mode	Software Mode	Hardware Mode	Software Mode	Hardware Mode	Software Mode	Hardware Mode	Software Mode
REFSEL	Yes	Yes						
SEQEN	Yes	No						
HW_RNGSELx (Range selection)			Yes	Yes			Yes	No
HW_RNGSEKx (Hardware or Software Mode)	Yes	Yes						
SER / $\overline{PAR}$	Yes	Yes						
OSx	Yes	No						
BURST	Yes	No						
CHSEL			Yes	No	Yes	No		
$\overline{SER1W}$	Yes	Yes						

1. Blank cell in Table 3 mean not applicable.

8.5 Software Mode

If software mode is selected and the reference voltage source and interface type are configured, all other configurations of the GD30AD33G0 must be set through the on-chip registers. When software mode is selected, all functions of the GD30AD33G0 are available. Table 3 summarizes the signals latched by the device when full reset is released, depending on the selected operating mode.

8.6 Reset Function

The GD30AD33G0 has two reset modes: full or partial. The reset mode selection depends on the length of the reset low pulse. A partial reset requires the $\overline{RESET}$ pin to be held low for 40 ns to 500 ns. After 50 ns of the $\overline{RESET}$ pin release, the device is fully available and conversions can be started. A full reset requires the $\overline{RESET}$ pin to be held low for at least 1.2 μs. After 15 ms of release $\overline{RESET}$ pin, the device has reconfigured and conversions can be started.

A partial reset reinitializes the following modules:

- Sequencer
- Digital Filter
- SPI
- Two SAR ADCs

When a partial reset is completed, the current conversion result is discarded. A partial reset does not affect register values set in software mode or latches that store user configurations in hardware and software mode. After a partial reset, a dummy conversion needs to be performed in software mode.

A full reset will reset the device to the default power-on state. When the GD30AD33G0 exits a full reset, the following configurations will be configured:

- Hardware mode or software mode
- Internal/external reference voltage source
- Interface Type

At power-up, the $\overline{\text{RESET}}$ signals can be released once both the V_{CC} and V_{DRIVE} supplies are stable. When the $\overline{\text{RESET}}$ pins are released after a full reset , the logic levels of the HW_RNGSELx, REFSEL, $\text{SER}/\overline{\text{PAR}}$ and $\text{DB4}/\overline{\text{SER1W}}$ pins determine the device configuration.

If hardware mode is selected, the functionality determined by the BURSTEN, SEQEN, and OSx signals is also latched when the RESET pin transitions from low to high in full reset mode. Once the functionality is configured, changes to these signals are ignored. In hardware mode, the analog input range (HW_RNGSELx signals) can be configured during full or partial reset or during normal operation, but the hardware/software mode selection requires a full reset to reconfigure and this setting is latched.

In hardware mode, the CHSELx and HW_RNGSELx pins are polled when exiting both full and partial resets to perform the following actions:

- Determines which initial analog input channel pair to acquire for conversion.
- Configure the initial settings of the sequencer.
- Selects the analog input voltage range.

The CHSELx and HW_RNGSELx signals are not latched. The channel pair or hardware sequencer to be converted can be reconfigured during normal operation by setting the CHSELx signal level before the rising edge of CONVST and maintaining it until BUSY goes low again. See the *Channel Selection* section for details.

In software mode, all other functions are configured through on-chip registers.

8.7 Pin Function Overview

GD30AD33G0 has several dual-function pins, whose functions depend on the operating mode selected by the HW_RNGSELx pin. The following table lists the pin functions in different operating modes and interface modes.

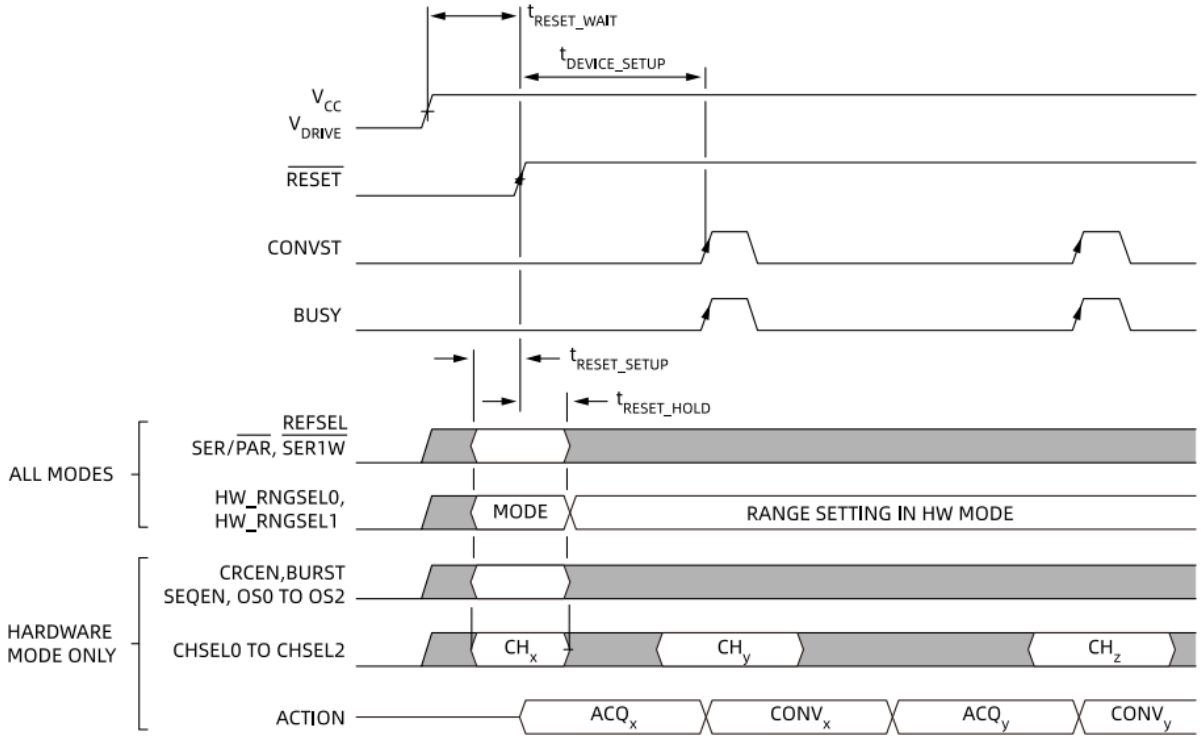


Figure 32. GD30AD33G0 Configuration During Reset

Table 4. Pin Function Overview

Pinout	Working Mode			
	Software mode, HW_RNGSELx = 00		Hardware mode, HW_RNGSELx ≠ 00	
	Serial, SER / $\overline{PAR}$ = 1	Parallel, SER / $\overline{PAR}$ = 0	Serial, SER / $\overline{PAR}$ = 1	Parallel, SER / $\overline{PAR}$ = 0
CHSEL	No function, connect to DGND	No function, connect to DGND	CHSEL	CHSEL
SCLK / $\overline{RD}$	SCLK	$\overline{RD}$	SCLK	$\overline{RD}$
$\overline{WR}$ / BURST	Connect to DGND	$\overline{WR}$	BURST	BURST
DB15/OS0 to DB13/OS2	Connect to DGND	DB15 to DB13	OSx	DB15 to DB13
DB12/SDOA	SDOA	DB12	SDOA	DB12
DB11/SDOB	SDOB, floating in serial 1-wire mode	DB11	SDOB	DB11
DB10/SDI	SDI	DB10	Connect to DGND	DB10
DB9 to DB6, DB3 to DB0	Connect to DGND	DB9 to DB6, DB3 to DB0	Connect to DGND	DB9 to DB6, DB3 to DB0
DB5	Connect to DGND	DB5		DB5
DB4 / $\overline{SER1WI}$	$\overline{SER1W}$	DB4	$\overline{SER1W}$	DB4
HW RNGSELX	HW RNGSELX, connect to DGND	HW RNGSELX, connect to DGND	HW RNGSELX, configure analog input range	HW RNGSELX, configure analog input range
SEOEN	No function, connect to	No function, connect to	SEQEN	SEQEN

Pinout	Working Mode			
	Software mode, HW_RNGSELx = 00		Hardware mode, HW_RNGSELx ≠ 00	
	Serial, SER / $\overline{PAR}$ = 1	Parallel, SER / $\overline{PAR}$ = 0	Serial, SER / $\overline{PAR}$ = 1	Parallel, SER / $\overline{PAR}$ = 0
	DGND	DGND		
REFSEL	REFSEL	REFSEL	REFSEL	REFSEL

9 Digital Interface

9.1 Channel Selection

9.1.1 Hardware Mode

The logic level of the CHSELx signal determines the channel pair to be converted; see Table 5. The CHSELx signal when exiting a full or partial reset determines the initial channel pair to be sampled. After reset, the logic level of the CHSELx signal is checked during the BUSY high period to set the channel pair for the next conversion. The CHSELx signal level must be set before CONVST changes from low to high and remains unchanged until BUSY changes from high to low, indicating that the conversion is complete.

9.1.2 Software Mode

In software mode, the channels to be converted are selected by the channel registers. At power-on or after reset, the default channels selected for conversion are V0A and V0B.

Table 5. CHSELx Pin Decoding

Channel Select Input Pin			Analog Input Channel to be Converted
CHSEL2	CHSEL1	CHSEL0	
0	0	0	V0A, V0B
0	0	1	V1A, V1B
0	1	0	V2A, V2B
0	1	1	V3A, V3B
1	0	0	V4A, V4B
1	0	1	V5A, V5B
1	1	0	V6A, V6B
1	1	1	V7A, V7B

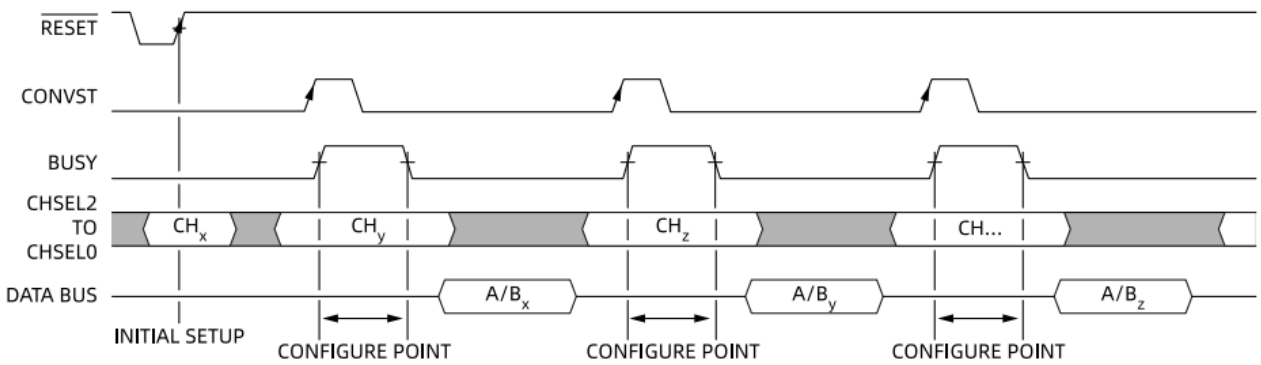


Figure 33. Hardware Mode Channel Conversion Settings

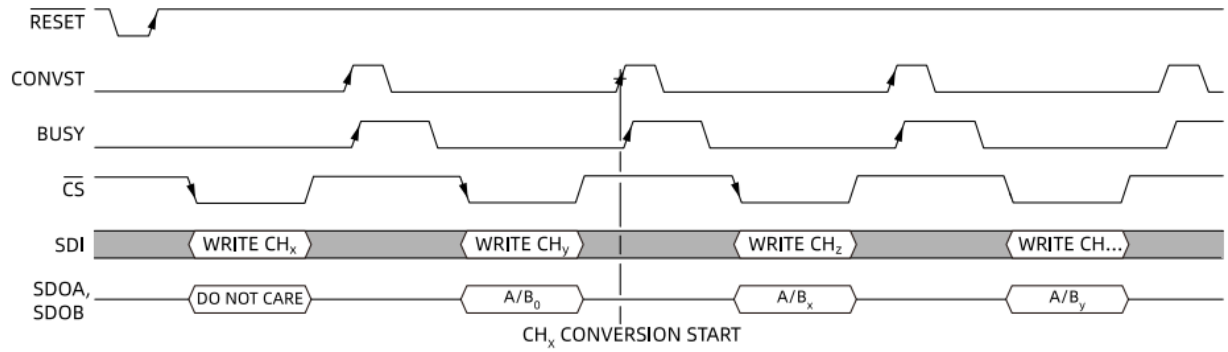


Figure 34. Software Serial Mode Channel Conversion Settings

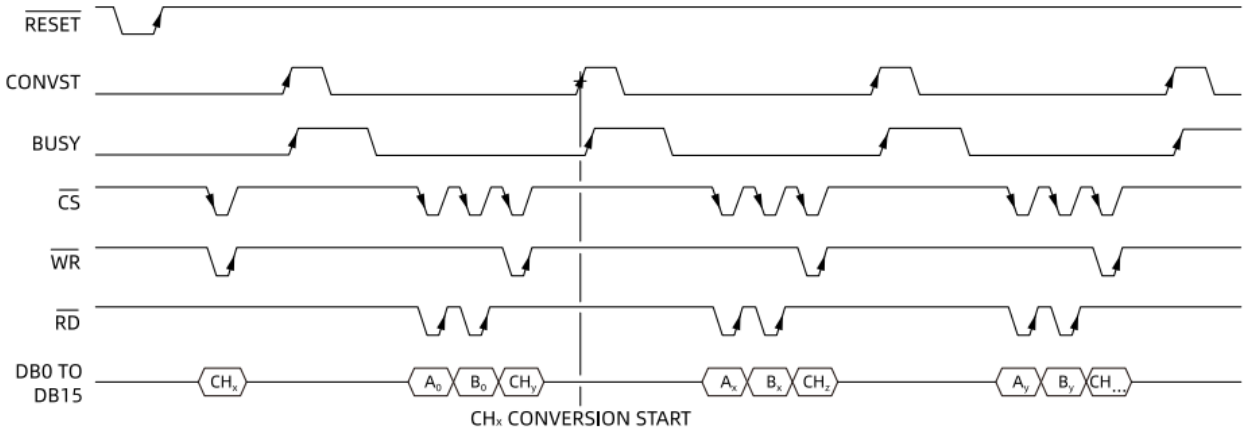


Figure 35. Software Parallel Mode Channel Conversion Settings

9.2 Parallel Interface

The parallel interface can be used to read conversion results, configure and read back on-chip registers. To read data from the GD30AD33G0, you can use the parallel data bus and use standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ signals. When reading data through the parallel bus, the $SER/\overline{PAR}$ pin needs to be connected to a low level.

9.2.1 Read the Conversion Result

The CONVST signal starts the conversion process. When the CONVST signal transitions from low to high, a conversion is initiated for the selected input. The BUSY signal transitions high to indicate that a conversion is in progress. The BUSY signal transitions from high to low to indicate that the conversion is complete and the result can be read back through the parallel interface.

To read data from the GD30AD33G0, you can use the parallel data bus and use the standard $\overline{CS}$ and $\overline{RD}$ signal. By internally selecting the $\overline{CS}$ and $\overline{RD}$ input signals , the conversion results can be output to the data bus. When $\overline{CS}$ and $\overline{RD}$ are both in the logic low state, the data lines DB15 to DB0 are out of the high impedance state.

GD30AD33G0 devices share the same parallel data bus. The rising edge of the $\overline{CS}$ input signal puts the bus into a tri-state, and the falling edge of the $\overline{CS}$ input signal takes the bus out of the high-impedance state. $\overline{CS}$ is the control signal that enables the data line; using this function, multiple required read operations are possible depending on the device configuration. For the A and B channels sampled simultaneously, at least two read

operations are required to read the conversion results. If other functions such as status and burst mode are enabled, the required readback times increase accordingly.

GD30AD33G0's $\overline{RD}$ pin is used to read data from the output conversion result register. Applying a series of $\overline{RD}$ pulses to the $\overline{RD}$ pins clocks the conversion results of each channel to be output one by one to the parallel bus DB15 to DB0. The first $\overline{RD}$ falling edge after BUSY goes low clocks out the conversion result of channel AX. The next $\overline{RD}$ falling edge updates the bus with the conversion result of channel BX.

To exit register mode in GD30AD33G0, data 0x0 needs to be written to address 0x00.

9.2.2 Write Register Data

In software mode, all read/write registers of the GD30AD33G0 can be written through the parallel interface. Through the parallel bus (DB15 to DB0), the GD30AD33G0 data is provided through the DB15 to DB0 inputs, with DB0 being the LSB of the data word. The format of the write command is shown in Figure 36. To select a write command, Bit D15 must be set to 1. Bits [D14:D9] are the register address. The following 9 bits (Bits [D8:D0]) contain the data to be written to the selected register. For a complete list of register addresses, see the "*Register Summary*" section. Data is accessed in a single 16-bit parallel access $\overline{WR}$ and $\overline{CS}$ signal to execute a register write command. The rising edge of the $\overline{WR}$, write is latched into the device.

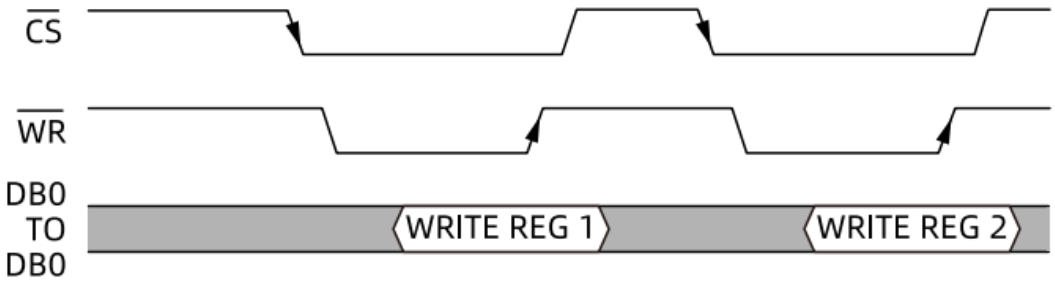


Figure 36. Parallel Interface Register Write Operation

9.2.3 Read Register Data

All registers in the device can be read through the parallel interface. To read a register, first write the address of the register to be read to the GD30AD33G0. The format of the register read command is shown in Figure 38. To select the read command, Bit D15 must be set to 0. Bits [D14:D9] are the register address. The following 9 bits (Bits [D8:D0]) are ignored. The read command is latched into the GD30AD33G0 on the rising edge of $\overline{WR}$. This latch will transfer the associated register data to the output register, and the register data can then be read through the DB15 to DB0 pins using a standard read command.

When reading a register, GD30AD33G0 bits [D14:D9] return the register address.

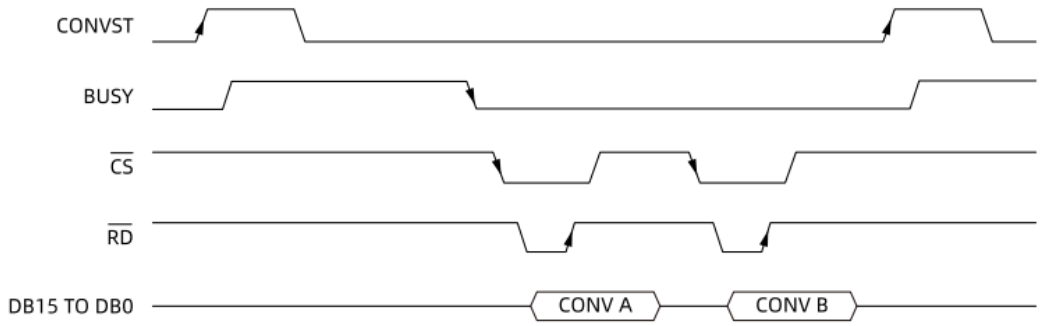


Figure 37. Parallel Interface Conversion Readback

Figure 38. Parallel Interface Register Read Operation

9.3 Serial Interface

To connect the GD30AD33G0 via SPI, the $\overline{\text{SER}}/\text{PAR}$ pin must be tied high. The $\overline{\text{CS}}$ and SCLK signal transmits data from the GD30AD33G0. The GD30AD33G0 has two serial data output pins: SDOA and SDOB. Use the Serial 1-wire or Serial 2-wire mode to read back data from the GD30AD33G0.

In the serial 2-wire mode of the GD30AD33G0, the conversion results of channels V0A to V7A appear on SDOA, and the conversion results of channels V0B to V7B appear on SDOB. In the serial 1-wire mode, the conversion results of channels V0B to V7B appear interleaved with the conversion results of channels V0A to V7A. To achieve the maximum throughput rate, use the 2-wire mode.

When reading back data through SDOA and SDOB, the $\overline{\text{SER1W}}$ pin must be tied high. When reading back data through SDOA only, the $\overline{\text{SER1W}}$ pin must be tied low. Serial 1-wire or 2-wire mode is configured when the GD30AD33G0 exits full reset.

9.3.1 Reading Conversion Results

The CONVST signal starts the conversion process. When the CONVST signal transitions from low to high, a conversion is initiated for the selected input. The BUSY signal transitions high to indicate that a conversion is in progress. The BUSY signal transitions from high to low to indicate that the conversion is complete and the conversion results can be read back through the serial interface.

The $\overline{\text{CS}}$ falling edge takes the data output lines SDOA and SDOB out of tri-state and outputs the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits into the serial data outputs, SDOA and SDOB. Figure 39 shows the use of two SDOx lines of the GD30AD33G0 to read two simultaneous conversion results. If the status register contents are appended to the conversion results, or if operating in sequencer burst mode (multiple 16 SCLK transfers to access data in the GD30AD33G0), it should be held low to frame all data. Data can also be output one by one using only one SDOx line, in which case SDOA must be used to access all

conversion data. When the GD30AD33G0 accesses the conversion results of two channels, VxA and VxB, via one SDOx line, a total of 32 SCLK cycles are required. The 32 SCLK cycle frames can be enabled with one $\overline{CS}$ signal, or the 16 SCLK cycle frames of each group can be enabled independently with $\overline{CS}$ signals. The disadvantage of using only one SDOx line is that the throughput rate is reduced.

In serial 1-wire mode, the unused SDOB line should be left unconnected. If SDOA is used as a single serial data output line, the channel results will be output in the following order: VxA and VxB. Figure 40 shows the 1-wire serial readback operation.

The data readback speed in serial interface mode depends on the SPI frequency, V_{DRIVE} supply, and the load capacitance C_{LOAD} on the SDO line. Table 6 lists the maximum speed achievable under different conditions.

Table 6. SPI Frequency vs. Load Capacitance and V_{DRIVE}

V_{DRIVE} (V)	C_{LOAD} (pF)	SPI frequency (MHz)
2.3 to 3	20	40
3 to 3.6	30	50

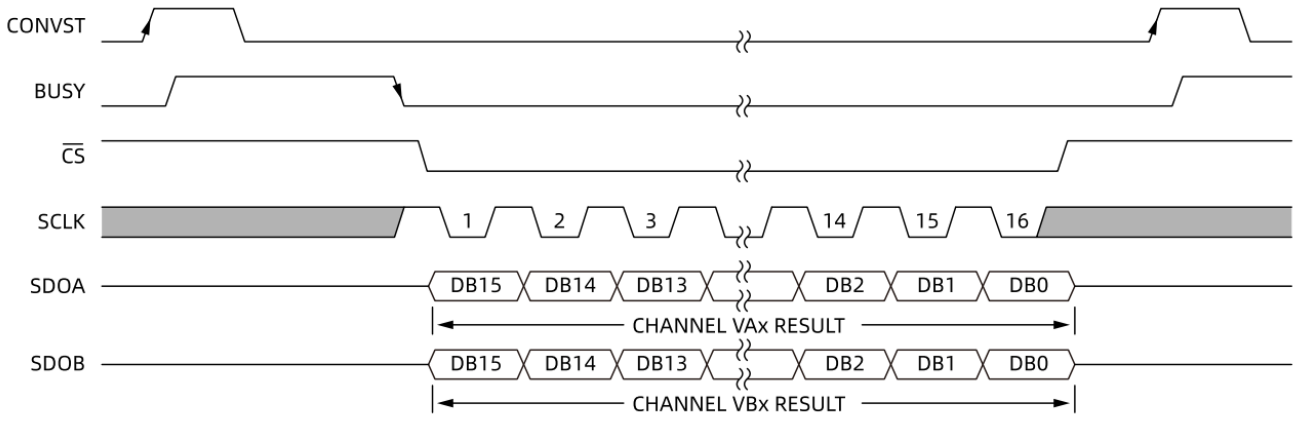


Figure 39. Serial Interface, 2-Wire Mode

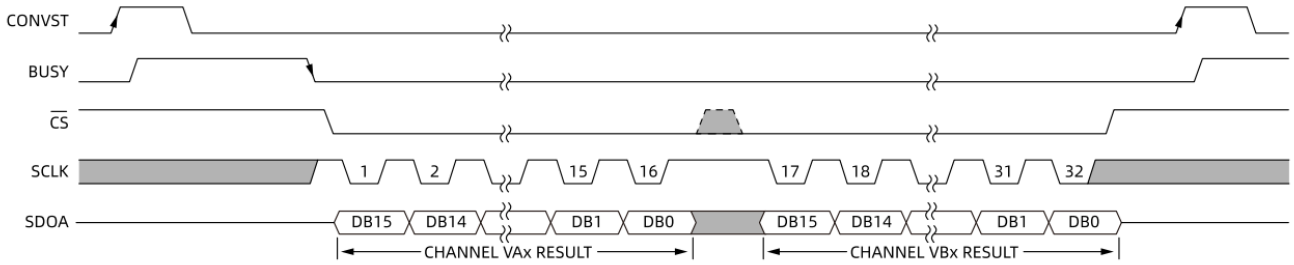


Figure 40. Serial Interface, 1-Wire Mode

9.3.2 Writing Register Data

All the read/write registers can be written in the GD30AD33G0 through the serial interface. Register write commands are executed through a single 16-bit SPI access. The format of the write command is shown in Table 7. To select a write command, Bit D15 must be set to 1. Bits [D14:D9] are the register address. The following 9 bits (Bits [D8:D0]) contain the data to be written to the selected register. Figure 41 shows a typical serial write command.

9.3.3 Reading Register Data

All registers in the device can be read through the serial interface. The command to read a register is executed by issuing a register read command followed by an additional SPI command; this command can be a valid command or a no operation (NOP). The format of the read command is shown in Table 8. Bit D15 must be set to 0 to select a read command. Bits [D14:D9] contain the register adress. The subsequent nine bits (Bits [D8:D0]) are ignored. See the *Register Summary* for a complete list of register addresses . Figure 42 shows a typical serial read command.

If the GD30AD33G0 is in register mode, SDO will read back the contents from the previously addressed register regardless of whether the previous frame was a read command or a write command. To exit register mode, write data 0x0 to address 0x00.

When reading a register, the bits [D14:D9] of GD30AD33G0 return the register address.

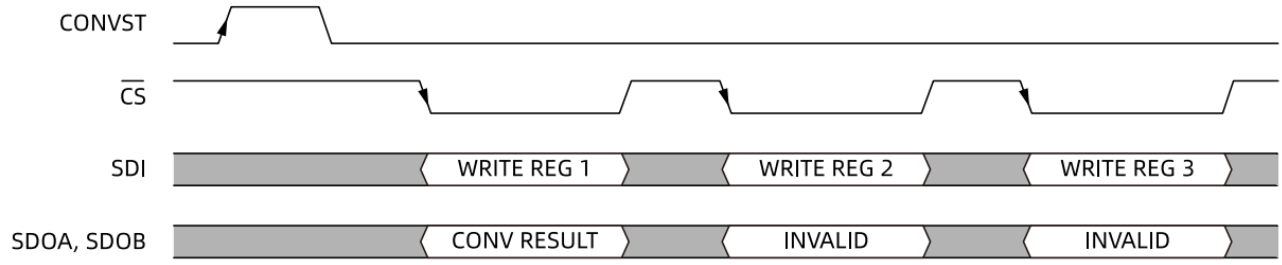


Figure 41. Serial Interface Register Write Operation

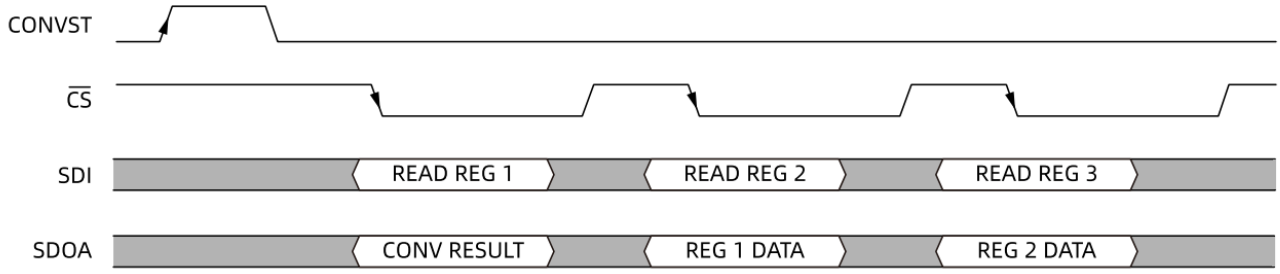


Figure 42. Serial Interface Register Write Operation

Table 7. Write Command Message Configuration

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/R	REGADDR[5:0]						Data[8:0]								
1	Register Address						Data to be written								

Table 8. Read Command Message Configuration

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/R	REGADDR[5:0]						Data[8:0]								
0	Register Address						Unrelated								

10 Sequencer

GD30AD33G0 has a highly configurable on-chip sequencer. The functionality and configuration of the sequencer depends on the operating mode of GD30AD33G0.

In hardware mode, the sequencer can only work in order, always starting with channels V0A and V0B, and then converting the subsequent channels in sequence until the last channel configured.

In software mode, the sequencer has additional features and configurations. The sequencer stack has 32 uniquely configurable sequence steps, allowing any channel order to be set. In addition, any channel VxA input can be paired with any channel VxB input or a diagnostic channel.

The sequencer can operate with or without the burst feature enabled. If the burst feature is enabled, only one CONVST pulse is required to convert all channels in a sequence. If the burst mode is disabled, a CONVST pulse is required for each conversion step in a sequence. For more information on burst mode operation, see the *Burst Sequencer*.

10.1 Hardware Mode Sequencer

In hardware mode, the sequencer is configured by the SEQEN pin and the CHSELx pins. When the GD30AD33G0 exits full reset, the sequencer is either enabled or disabled. When the RESET pin is released, the logic level of the SEQEN pin determines whether the sequencer is enabled or disabled. After releasing the $\overline{\text{RESET}}$ pin, the function is fixed, and to exit the function and set another configuration, a full reset is required through the $\overline{\text{RESET}}$ pin.

Table 9. Hardware Mode Sequencer Configuration

SEQEN	Interface Mode
0	Disable Sequencer
1	Enable sequencer

When the sequencer is enabled, the logic level of the CHSELx pin determines which channels are selected for conversion in the sequence. The state of the CHSELx pin when the $\overline{\text{RESET}}$ pin is released determines the initial settings of the channels to be converted in the sequence. To later reconfigure the channels selected for conversion, set the CHSELx pin to the desired setting for the duration of the last BUSY pulse before the current conversion sequence is completed. See Figure 43.

Table 10. CHSELx Pin Decode Sequencer

Channel select input pin			Analog input channels to be converted sequentially
CHSEL0	CHSEL1	CHSEL2	
0	0	0	V0x only
0	0	1	V0x to V1x
0	1	0	V0x to V2x
0	1	1	V0x to V3x
1	0	0	V0x to V4x
1	0	1	V0x to V5x
1	1	0	V0x to V6x
1	1	1	V0x to V7x

10.2 Software Pattern Sequencer

In software mode, the GD30AD33G0 contains a 32-layer fully configurable sequencer stack. The sequencer can be controlled by writing configuration registers and sequencer stack registers through the parallel or serial interface.

Each stack step can be configured independently, any input of channel VxA can be paired with any input of channel VxB, or any diagnostic channel can be selected for conversion. The sequencer depth can be set from 1 to 32 levels. The sequencer depth is controlled by the SSRENx bits. Set the SSRENx bits in the sequencer stack register according to the desired final step. For the desired depth, select the channel to be converted by writing the ASELx and BSELx bits in each sequencer stack register.

Setting the SEQEN bit in the configuration register to 1 activates the sequencer.

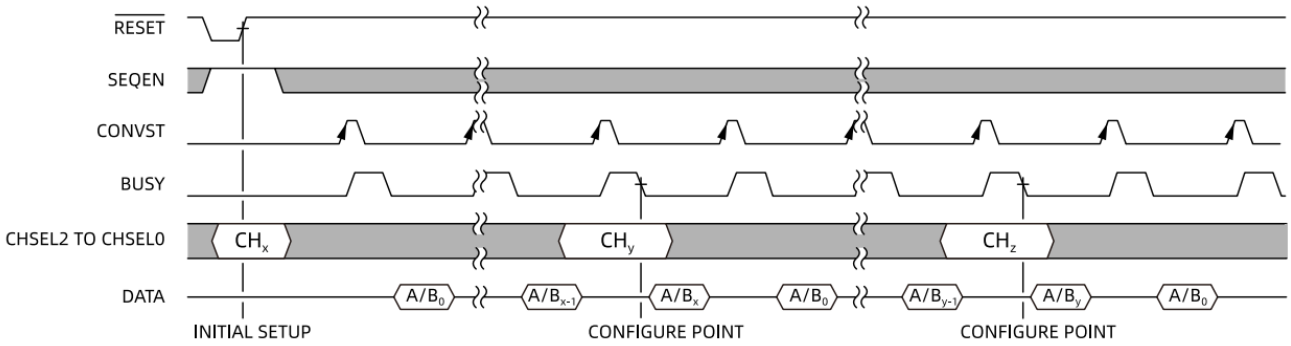


Figure 43. Hardware Mode Sequencer Configuration

To configure and enable the sequencer, the following steps are recommended:

1. Configure the analog input range for the desired analog input channels.
2. Set the sequencer stack registers to select the channels in the sequence.
3. Set the SSRENx bit in the desired last sequence step.
4. Set the SEQEN bit in the configuration register.
5. Write data 0x0 to address 0x00 to exit register mode.
6. Provide a dummy CONVST pulse.
7. Repeatedly send the CONVST pulse and read the conversion results, stepping through each element in the sequencer stack.

If another CONVST pulse comes, the sequence will automatically restart from the first element in the sequencer stack. After a partial reset, the sequencer pointer is repositioned at the first level of the stack, but the register settings remain unchanged.

10.3 Burst Sequencer

In burst mode, it is not necessary to generate a CONVST pulse for each step in the conversion sequence. One CONVST pulse can convert each step in the sequence.

The burst sequencer is an additional feature that works in conjunction with the sequencer. If the burst feature is enabled, a single CONVST pulse starts the conversion of all channels configured in the sequencer. When using the burst feature, it is not necessary to generate a CONVST pulse for each step in the conversion sequence, as is the case if the burst feature is disabled.

The configuration of the burst feature depends on the operating mode: hardware mode or software mode. For specific information on configuring the burst feature in each mode, refer to the *Hardware Mode* section and the *Software Pattern Sequencer* section.

Once configured, the burst sequence is initiated on the rising edge of CONVST. The BUSY pin goes high to indicate that a conversion is in progress. The BUSY pin will remain high until all conversions in the sequence have completed. After the BUSY pin goes low, the conversion results can be read back.

The number of data reads required to read all the data in a burst sequence depends on the configured sequence length.

The conversion results appear on the data bus (parallel or serial) in the order in which the channels are set.

In burst mode, the throughput rate of the GD30AD33G0 is limited, and the specific value depends on the sequence length. Each channel pair requires acquisition, conversion, and readback time. The time required to complete a sequence containing N pairs of channels can be estimated by the following formula:

$$t_{BURST} = (t_{CONV} + 25ns) + (N-1)(t_{ACQ} - t_{CONV}) + N(t_{RB}) \quad (1)$$

Where:
t_{CONV} is the typical conversion time.
t_{ACQ} is the typical acquisition time.
t_{RB} is the time required to read back the conversion result in Serial 1-Wire, Serial 2-Wire, or Parallel mode.

10.3.1 Hardware Mode Burst

Burst mode is enabled in hardware mode by setting the BURST pin to 1. Also set the SEQEN pin to 1 to enable the sequencer.

In hardware mode, the burst sequencer is configured by the BURST, SEQEN, and CHSELx pins. When the GD30AD33G0 exits full reset, the burst sequencer is either enabled or disabled. When the RESET pin is released, the logic levels of the SEQEN pin and the BURST pin determine whether the burst sequencer is enabled or disabled. After releasing the RESET pin, the function is fixed, and to exit the function and set another configuration, a full reset is required through the RESET pin.

When the burst sequencer is enabled, the logic level of the CHSELx pin determines which channels are selected for conversion in the burst sequence. The state of the CHSELx pin when the RESET pin is released determines the initial setting of channels to be converted in the sequence. To reconfigure the channels selected for conversion after a reset, set the CHSELx pin to the desired setting for the next BUSY pulse (see Figure 45).

10.3.2 Software Mode Burst

In software mode, the burst feature is enabled by setting the BURST bit in the configuration register to 1. This must be done by setting the SEQEN bit in the configuration register to 1, as described in the steps to configure the sequencer in the *Software Pattern Sequencer* section (see Figure 46).

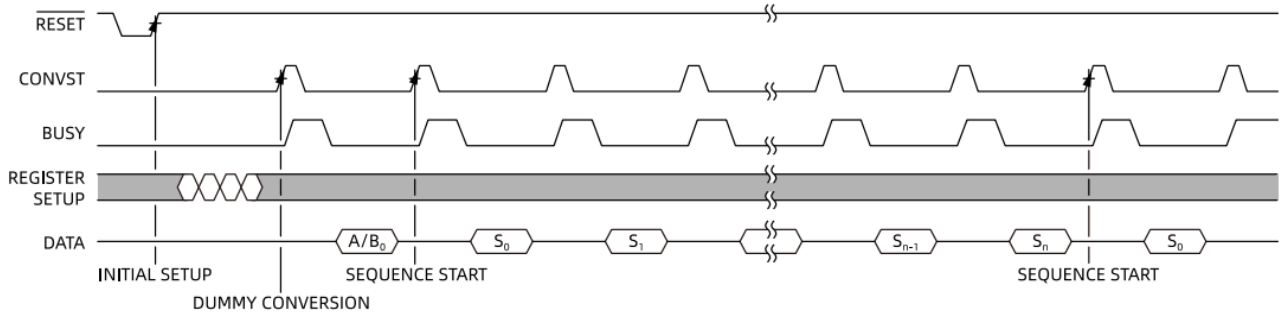


Figure 44. Software Mode Sequencer Configuration

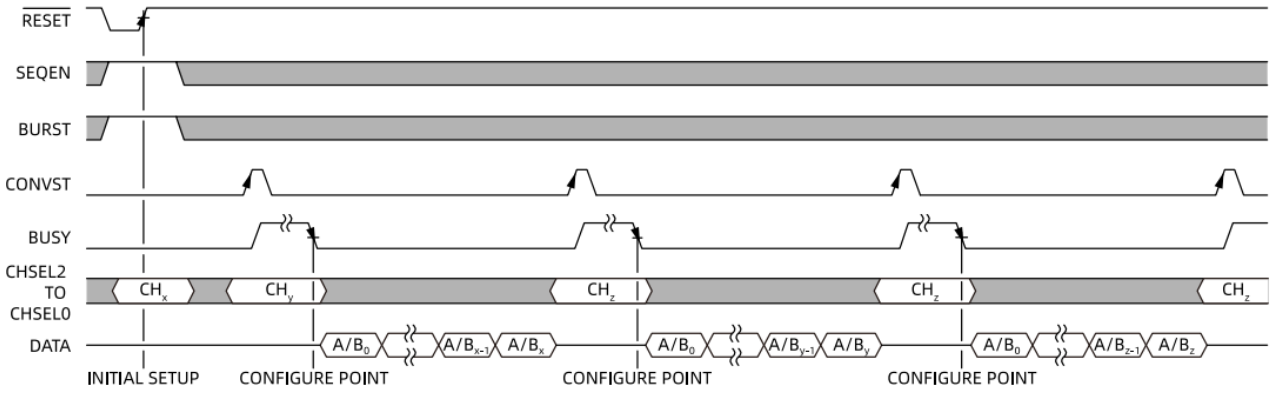


Figure 45. BURST Sequencer Hardware Mode

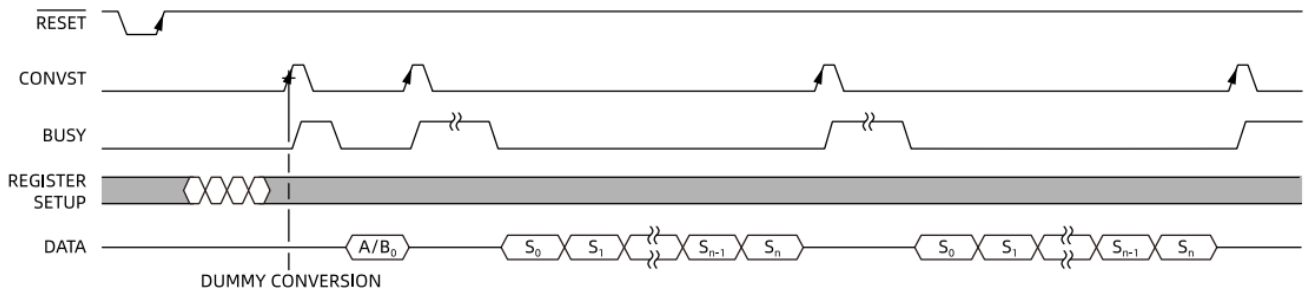


Figure 46. BURST Sequencer Software Mode

In burst sequencer mode, GD30AD33G0 can only pull down the $\overline{CS}$ signal once to read all channel data of the sequencer.

11 Diagnosis

11.1 Diagnostic Channel

In addition to the 16 analog inputs VxA and VxB, the GD30AD33G0 can also convert the following diagnostic channels: VCC and analog ALDO voltage. The diagnostic channel can be selected for conversion by setting the channel register (see the " *Channel Register*" section) to the corresponding channel identifier. Diagnostic channels can also be added to the sequencer stack in software mode, but to provide accurate readings, the throughput rate must be less than 250 kSPS. Figure 47 shows the relationship between the deviation from the expected value and the sampling frequency when the diagnostic channel is used.

The expected output of each channel is determined by the following transfer function: Where V_{REF} is the voltage on the REFCAP pin, which has a typical value of 4.096V.

$$V_{CC}Code=\frac{\left[\left(4\times V_{CC}\right)-V_{REF}\right]\times 32768}{5\times V_{REF}} \quad (2)$$

$$LDO\,Code=\frac{\left[\left(10\times V_{ALDO}\right)-\left(7\times V_{REF}\right)\right]\times 32768}{10\times V_{REF}} \quad (3)$$

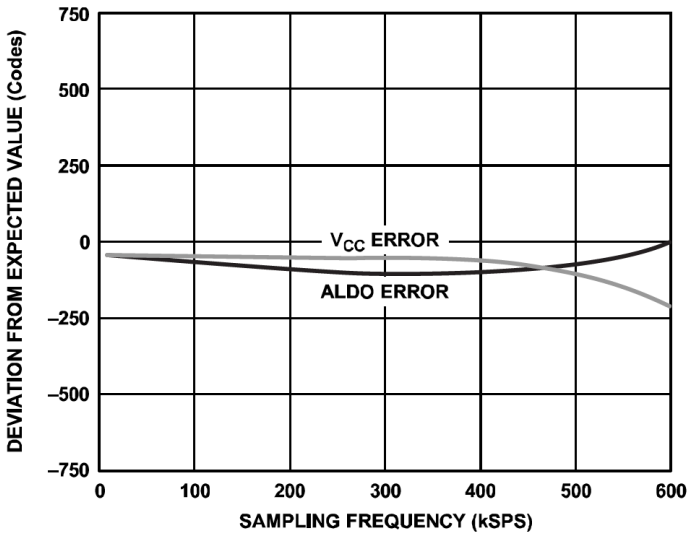


Figure 47. Deviation from Expected Value vs. Sampling Frequency

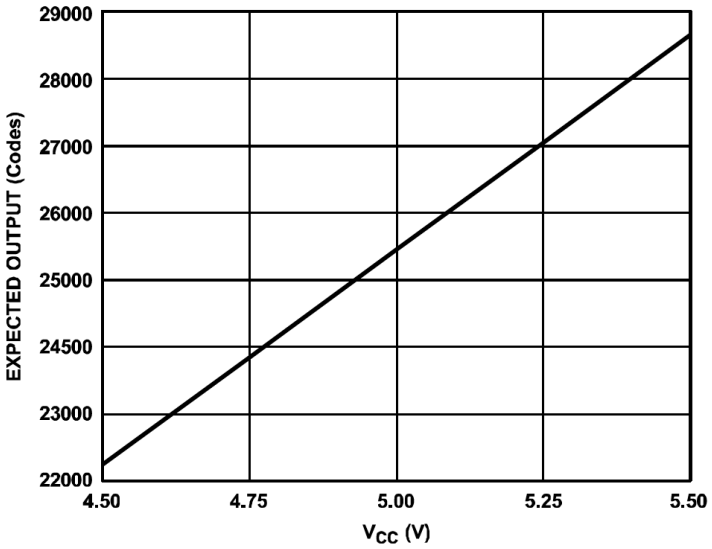


Figure 48. V_{CC} Diagnostic Transfer Function

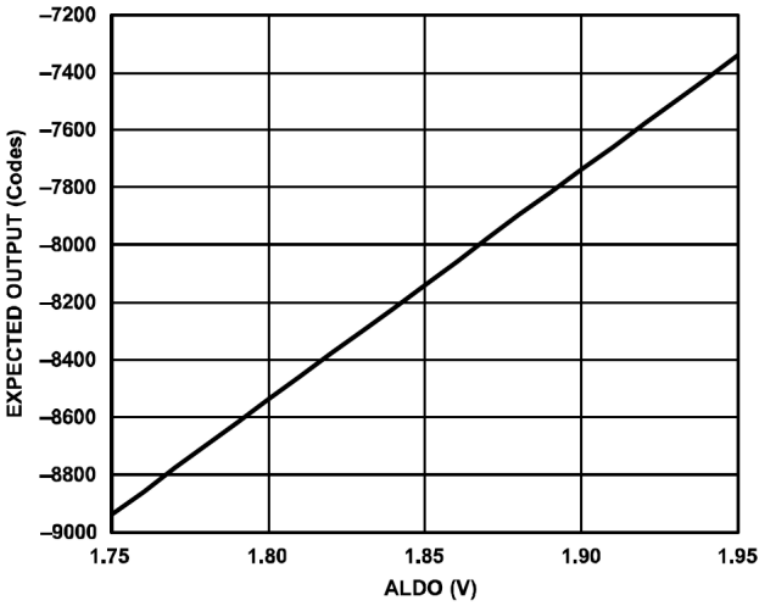


Figure 49. ALDO Diagnostic Transfer Function

11.2 Interface Self-Test

The integrity of the digital interface can be tested by selecting the communication self-test channel in the channel register (see the " *Channel Register*" section).

The configuration register selects the communication self-test channel and performs a conversion (a dummy conversion is required for the first time in non-sequencer mode), which forces the conversion result register to a known fixed output. When reading the conversion code, the code 0xAAAA is output as the conversion code of ADC A, and the code 0x5555 is output as the conversion code of ADC B.

11.3 CRC

GD30AD33G0 features a Cyclic Redundancy Check (CRC) mode, which can detect errors in the data, thereby enhancing the robustness of the interface. The CRC feature can be used in both software (serial and parallel) modes and hardware (only serial) modes. The CRC feature cannot be used in hardware parallel mode. The CRC result is included in the status register. Enabling the CRC feature also enables the status register, and vice versa.

In hardware mode, the CRCEN pin controls the CRC feature. When GD30AD33G0 exits full reset, the CRC feature is either enabled or disabled. The logic level of the CRCEN pin when the $\overline{\text{RESET}}$ pin is released determines whether the CRC feature is enabled or disabled. When the CRCEN pin is set to 1, the CRC feature is enabled. Once the $\overline{\text{RESET}}$ pin is released, this function is fixed, and to exit this feature and set another configuration, a full reset through the $\overline{\text{RESET}}$ pin is required. More information can be found in the "Reset Function" section. After enabling, the CRC result is appended to the conversion result. The CRC status register is a 16-bit word, with the first 8 bits being the channel ID of the last conversion channel pair and the last 8 bits being the CRC result. This result is accessed through an additional read command, as shown in Figure 50.

In software mode, setting the CRCEN bit or the STATUSEN bit to 1 in the configuration register enables the CRC function (see "Configuration Register" section).

After enabling the CRC function, the conversion results of channel VxA and channel VxB are calculated for CRC. Depending on the device configuration, after the conversion result is transmitted, the CRC is calculated and transmitted through the serial or parallel interface. The Hamming distance is related to the number of bits in the conversion result. When the number of bits in the conversion result is ≤119, the Hamming distance is 4. When the number of bits is >119, the Hamming distance is 1, meaning that 1-bit errors will always be detected.

The following pseudocode illustrates how CRC is implemented in GD30AD33G0:

```
crc = 8'b0;
i = 0;
x = number of conversion channel pairs;
for (i=0, i<x, i++) begin
crc1 = crc_out(An,Crc);
crc = crc_out(Bn,Crc1);
i = i +1;
end
where crc_out(data, crc) :
crc_out[0] = data[14] ^ data[12] ^ data[8] ^data[7] ^ data[6] ^ data[0] ^ crc[0] ^crc[4] ^ crc[6];
crc_out[1] = data[15] ^ data[14] ^ data[13]^ data[12] ^ data[9] ^ data[6] ^ data[1] ^data[0] ^ crc[1] ^ crc[4] ^ crc[5]
^ crc[6]^ crc[7];
crc_out[2] = data[15] ^ data[13] ^ data[12]^ data[10] ^ data[8] ^ data[6] ^ data[2] ^data[1] ^ data[0] ^ crc[0] ^ crc[2]
^ crc[4]^ crc[5]
^ crc[7];
crc_out[3] = data[14] ^ data[13] ^ data[11]^ data[9] ^ data[7] ^ data[3] ^ data[2] ^data[1] ^ crc[1] ^ crc[3] ^ crc[5] ^
crc[6];
crc_out[4] = data[15] ^ data[14] ^ data[12]^ data[10] ^ data[8] ^ data[4] ^ data[3] ^data[2] ^ crc[0] ^ crc[2] ^ crc[4]
^ crc[6]^ crc[7];
crc_out[5] = data[15] ^ data[13] ^ data[11]^ data[9] ^ data[5] ^ data[4] ^ data[3] ^crc[1] ^ crc[3] ^ crc[5] ^ crc[7];
```

crc_out[6] = data[14] ^ data[12] ^ data[10]^ data[6] ^ data[5] ^ data[4] ^ crc[2] ^crc[4] ^ crc[6];
crc_out[7] = data[15] ^ data[13] ^ data[11]^ data[7] ^ data[6] ^ data[5] ^ crc[3] ^crc[5] ^ crc[7];

The initial CRC word used by GD30AD33G0 is an 8-bit word equal to 0. The XOR operation described in the code above is used to calculate the CRC word for each bit of the conversion result AN. Then, this CRC word (crc1) is used as the starting point for the calculation of the CRC word (crc) for the conversion result BN. For each pair of converted channels, the process described above is repeated in a loop.

Depending on the operating mode of GD30AD33G0, the status register value is appended to the conversion data and read out through the serial or parallel interface using an additional read command. Then, for the received conversion result, the user can repeat the XOR calculation described in the code above to check if the two CRC words are consistent. Figure 50 shows how the CRC word is appended to the data in each operating mode.

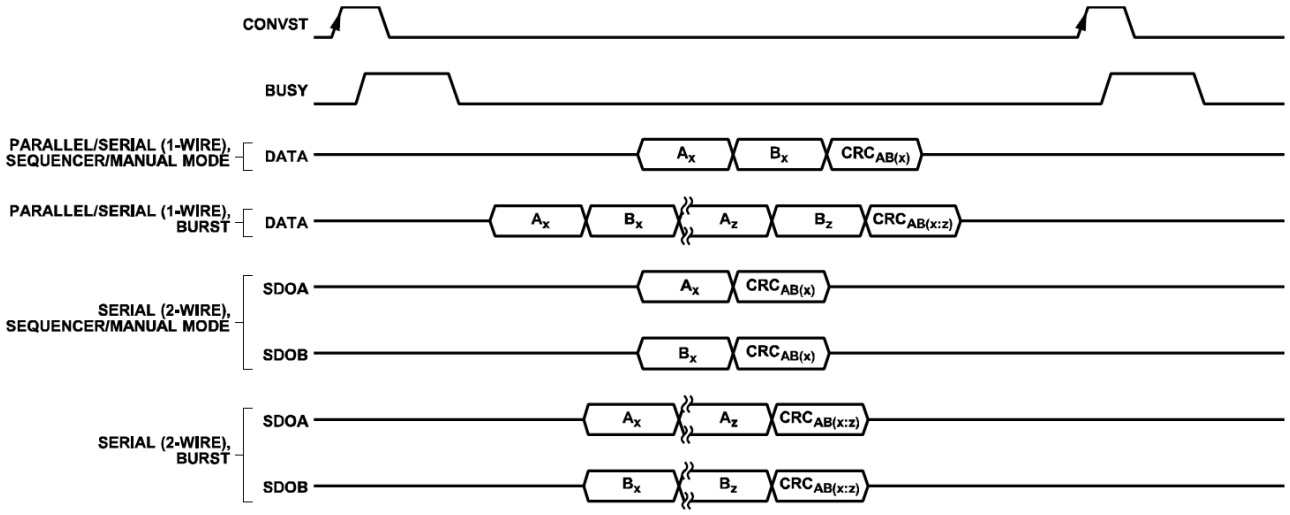


Figure 50. CRC Callback in All Modes

12 Register Summary

The GD30AD33G0 has six read/write registers for configuring the device in software mode, 32 sequencer stack registers for setting the flexible on-chip sequencer, and a read-only status register. Table 11 is a list of the read/write registers of the GD30AD33G0. The status register is a read-only register that contains information about the channel pair that was last converted.

Table 11. Register Summary[1]

Register	Name	Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02	Configuration Registers	[15:8]	Addressing							reserve	0x0000	R/W
		[7:0]	SDEF	BURSTEN	SEQEN	OS			STATUSEN	reserve		
0x03	Configuration Registers	[15:8]	Addressing							reserve	0x0000	R/W
		[7:0]	CHB				CHA					
0x04	Input Range Register A1	[15:8]	Addressing							reserve	0x00FF	R/W
		[7:0]	V3A		V2A		V1A		V0A			
0x05	Input Range Register A2	[15:8]	Addressing							reserve	0x00FF	R/W
		[7:0]	V7A		V6A		V5A		V4A			
0x06	Input range register B1	[15:8]	Addressing							reserve	0x00FF	R/W
		[7:0]	V3B		V2B		VB1		V0B			
0x07	Input range register B2	[15:8]	Addressing							reserve	0x00FF	R/W
		[7:0]	V7B		V6B		VB5		V4B			
0x20 to 0x3F	Sequencer Stack Registers [0:31]	[15:8]	Addressing							SSRENx	0x0000[2]	R/W
		[7:0]	BSELx				ASEL					
N/A	Status Register	[15:8]	A[3:0]				B[3:0]				N/A	R
		[7:0]	Reserved [7:0]									

1. N/A means not applicable.
2. After a full or partial reset is initiated, the sequencer stack registers are reinitialized, traversing from Channel V0A and Channel V0B to Channel V7A and Channel V7B and looping. The remaining 24 levels of the stack are reinitialized to 0x0.

12.1 Addressing Register

The seven MSBs written to the device are used to determine the register to be addressed. The seven MSBs consist of the register address (REGADDR) bits [5:0] and the read/write bit. The register address bits determine which on-chip register is selected. The read/write bit determines whether the remaining nine bits of data on the DB10/SDI line are loaded into the addressed register. If the read/write bit is 1, these bits are loaded into the register addressed by the register select bits. If the read/write bit is 0, the command is considered a read operation request. The addressed register data can be read in the next read operation.

MSB

D15	D14	D13	D12	D11	D10	D9	D8 to D0
W/R	REGADDR[5]	REGADDR[4]	REGADDR[3]	REGADDR[2]	REGADDR[1]	REGADDR[0]	DATA[8:0]

Table 12. Addressing Register Configuration Description

Bits	Pin Name	Description
D15	W/R	If 1 is written to this bit, bits [D8:D0] of this register are written to the register specified by REGADDR [5:0]. If 0 is written, the next operation is to read the specified register.
D14	REGADDR[5]	If a 1 is written to this bit, the contents of REGADDR [4:0] specify the 32 sequencer stack registers. If a 0 is written to this bit, the register defined by REGADDR[4:0] is selected.
[D13:D9]	REGADDR[4:0]	When W/R = 1, the contents of REGADDR[4:0] determine the register to be selected as follows: 00001: Reserved. 00010: Select configuration register. 00011: Select channel register. 00100: Select input range register A1. 00101: Select input range register A2. 00110: Select input range register B1. 00111: Select input range register B2. 01000: Select status register. When W/R = 0, REGADDR[4:0] is 00000 and the conversion code is read.
[D8:D0]	DATA[8:0]	Write these bits to the register specified by bits REGADDR [5:0]. See the following sections for a detailed description of each register.

12.2 Configuration Registers

The configuration registers are used in software mode to configure many of the key features of the ADC, including the sequencer, burst mode, oversampling, and retention options.

Address: 0x02; Reset: 0x0000; Name: Configuration Register

Table 13. Configuration Register Bit Description

Bit	Bit Name	Settings	Description	Reset[1]	Access
[15:9]	Addressing	0	Bits [15:9] specify the address of the associated register. See the *Addressing Register* section for more details.	0x0	RW
8	Reserve		Reserve.	0x0	R/W
7	SDEF		Self-test error flag.	N/A	R
		0	The test passed. GD30AD33G0 successfully completed its self-configuration after powering on.		
		1	Test failed. Problem detected during device configuration. Reset required.		
6	BURSTEN		Burst mode enabled.	0x0	RW
		0	Burst mode is disabled. A CNVST pulse is required for each channel pair to be converted.		
		1	A single CNVST pulse converts each channel pair set in the 32-layer sequencer stack register, up to and including the layer defined by the SSRENx bits. See the *Software Pattern Sequencer* section and *Software Mode Burst* section for more details.		
5	SEQEN		Channel sequencer enable.	0x0	RW
		0	Disable the channel sequencer.		
		1	Enable the channel sequencer.		
[4:2]	OS		Oversampling (OS) ratio, number of samples per channel.	0x0	RW
		000	Disable oversampling.		
		001	Oversampling enabled, OSR = 2.		
		010	Oversampling enabled, OSR = 4.		
		011	Oversampling enabled, OSR = 8.		
		100	Oversampling enabled, OSR = 16.		
		101	Oversampling enabled, OSR = 32.		
		110	Oversampling enabled, OSR = 64.		
		111	Oversampling enabled, OSR = 128.		
1	STATUSEN		Status register output enable.	0x0	RW
		0	When reading the conversion results, the status register is not read out.		
		1	After reading out all conversion words for all selected channels (including the self-test channels if enabled in sequencer mode), read out the status register.		
0	CRCEN		CRC enable. The STATUSEN and CRCEN bits have identical functionality.	0x0	RW

1. N/A means not applicable.

12.3 Channel Register

Address: 0x03; Reset: 0x0000; Name: Channel Register

In software manual mode, the channel register selects the input channel or self-test channel for the next conversion.

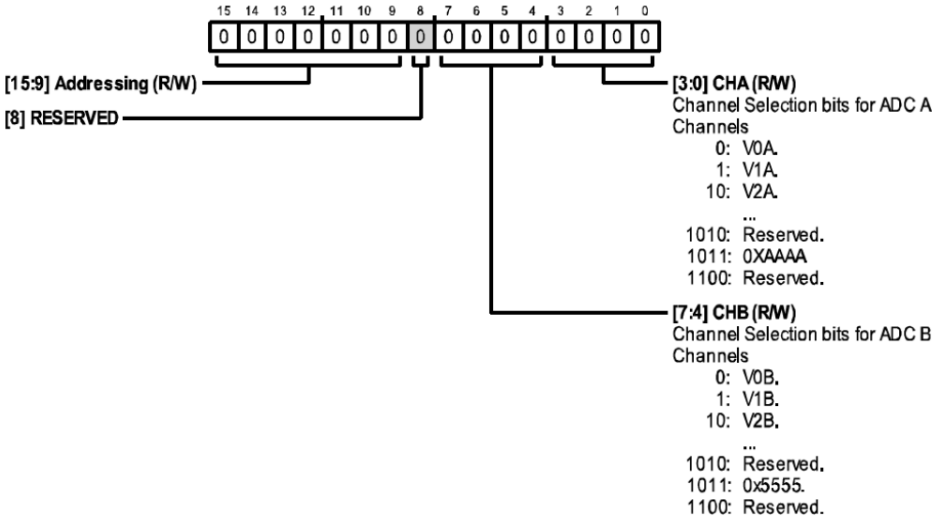


Table 14. Channel Register Bit Function Description

Bit	Bit Name	Setting	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] specify the address of the associated register. See the Addressing Registers section for more details.	0x0	R/W
8	reserve		reserve.	0x0	R/W
[7:4]	CHB		Channel select bits for ADC B channel.		
		0000	V0A/V0B.		
		0001	V1A/V1B.		
		0010	V2A/V2B.		
		0011	V3A/V3B.		
		0100	V4A/V4B.		
		0101	V5A/V5B.		
		0110	V6A/V6B.		
		0111	V7A/V7B.		
		1000	VCC		
		1001	ALDO		
		1010	reserve.		
		1011	Set the dedicated bit for the digital interface communication self-test function. When reading the transition code, the code 0xAAAA is read out as the transition code of channel A, and the code 0x5555 is read out as the transition code of channel B.		

Bit	Bit Name	Setting	Description	Reset	Access
		1100	reserve.		
[3:0]	CHA		Channel select bit for ADC A channel. Same settings as ADC B.	0x0	R/W

12.4 Input Range Register

Input Range Register A1 and Input Range Register A2 select one of three possible input ranges (±10V, ±5V, or ±2.5V) for analog input channels V0A to V7A. Input Range Register B1 and Input Range Register B2 select one of three possible input ranges (±10V, ±5V, or ±2.5V) for analog input channels V0B to V7B.

12.4.1 Input Range Register A1

Address: 0x04; Reset: 0x00FF; Name: Input range register A1.

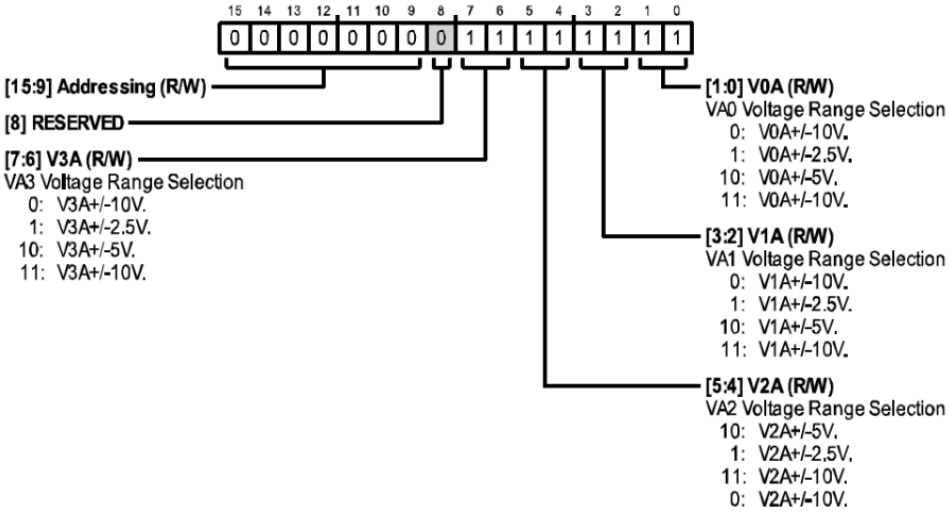


Table 15. Bit Description of Input Range Register A1

Bit	Bit Name	Setting	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] specify the address of the associated register. See the *Addressing Register* section for more details.	0x0	R/W
8	reserved		reserved.	0x0	R/W
[7:5]	V3A		V3A voltage range selection.	0x3	R/W
		00	V3A ± 10V.		
		01	V3A ± 2.5V.		
		10	V3A ±5V.		
		11	V3A ± 10V.		
[5:4]	V2A		V2A voltage range selection.	0x3	R/W
		00	V2A ± 10V.		
		01	V2A ± 2.5V.		
		10	V2A ±5V.		
		11	V2A ± 10V.		
	V1A		V1A voltage range selection.	0x3	R/W

Bit	Bit Name	Setting	Description	Reset	Access
[3:2]		00	V1A ± 10V.		
		01	V1A ± 2.5V.		
		10	V1A ±5V.		
		11	V1A ± 10V.		
[1:0]	V0A		V0A voltage range selection.	0x3	R/W
		00	V0A ± 10V.		
		01	V0A ± 2.5V.		
		10	V0A ±5V.		
		11	V0A ± 10V.		

12.4.2 Input Range Register A2

Address: 0x05; Reset: 0x00FF; Name: Input range register A2.

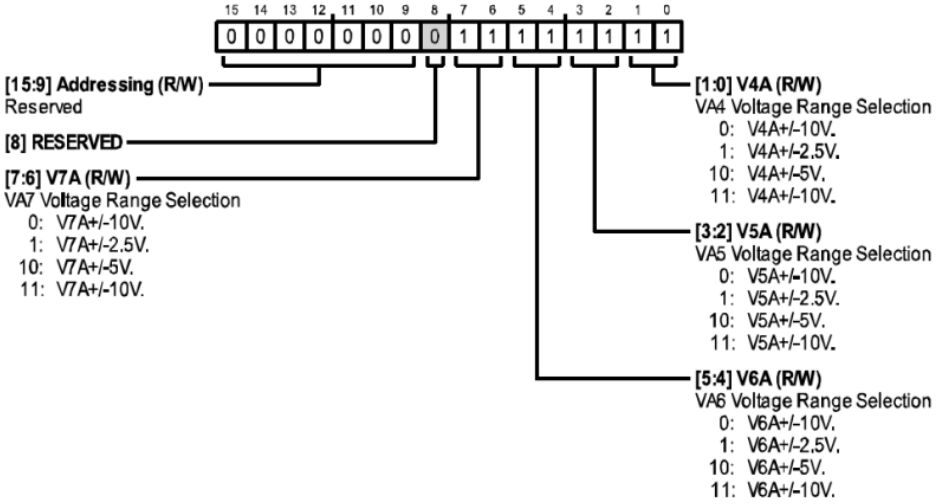


Table 16. Bit Description of Input Range Register A2

Bit	Bit Name	Setting	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] specify the address of the associated register. See the *Addressing Register* section for more details.	0x0	R/W
8	reserved		reserved.	0x0	R/W
[7:5]	V7A		V7A voltage range selection.	0x3	R/W
		00	V7A ± 10V.		
		01	V7A ± 2.5V.		
		10	V7A ±5V.		
		11	V7A ± 10V.		
[5:4]	V6A		V6A voltage range selection.	0x3	R/W
		00	V6A ± 10V.		
		01	V6A ± 2.5V.		

Bit	Bit Name	Setting	Description	Reset	Access
		10	V6A ±5V.		
		11	V6A ± 10V.		
[3:2]	V5A		V5A voltage range selection.	0x3	R/W
		00	V5A ± 10V.		
		01	V5A ± 2.5V.		
		10	V5A ±5V.		
		11	V5A ± 10V.		
[1:0]	V4A		V4A voltage range selection.	0x3	R/W
		00	V4A ± 10V.		
		01	V4A ± 2.5V.		
		10	V4A ±5V.		
		11	V4A ± 10V.		

12.4.3 Input Range Register B1

Address: 0x06; Reset: 0x00FF; Name: Input range register B1.

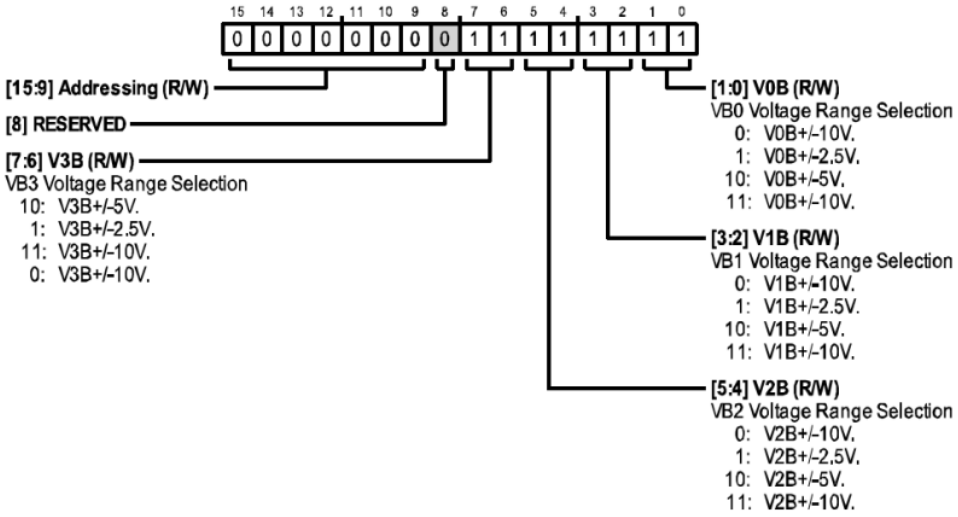


Table 17. Bit Description of Input Range Register B1

Bit	Bit Name	Setting	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] specify the address of the associated register. See the *Addressing Register* section for more details.	0x0	R/W
8	reserved		reserved.	0x0	R/W
[7:5]	V3B		V3B voltage range selection.	0x3	R/W
		00	V3B ± 10V.		
		01	V3B ± 2.5V.		
		10	V3B ±5V.		
		11	V3B ± 10V.		
[5:4]	V2B		V2B voltage range selection.	0x3	R/W
		00	V2B ± 10V.		

Bit	Bit Name	Setting	Description	Reset	Access
		01	V2B ± 2.5V.		
		10	V2B ±5V.		
		11	V2B ± 10V.		
[3:2]	V1B		V1B voltage range selection.	0x3	R/W
		00	V1B ± 10V.		
		01	V1B ± 2.5V.		
		10	V1B ±5V.		
		11	V1B ± 10V.		
[1:0]	V0B		V0B voltage range selection.	0x3	R/W
		00	V0B ± 10V.		
		01	V0B ± 2.5V.		
		10	V0B ±5V.		
		11	V0B ± 10V.		

12.4.4 Input Range Register B2

Address: 0x07; Reset: 0x00FF; Name: Input range register B2.

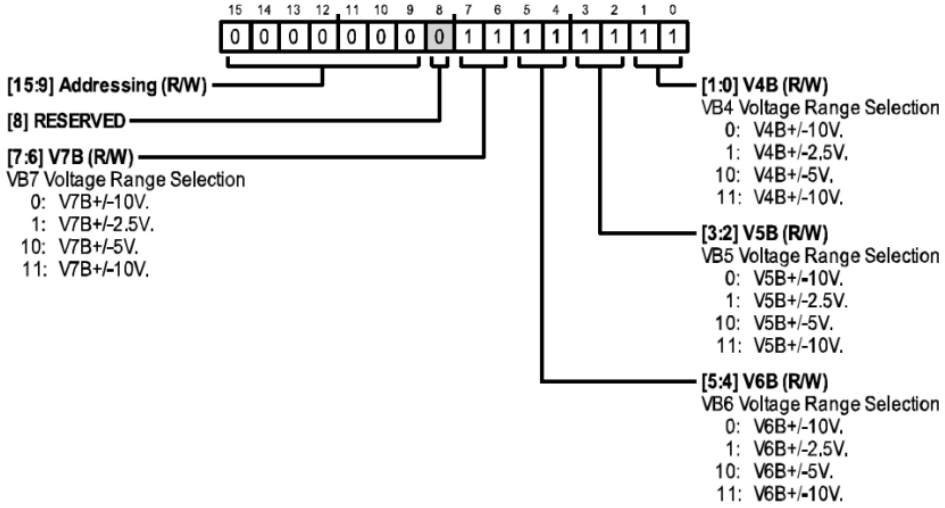


Table 18. Bit Description of Input Range Register B2

Bit	Bit Name	Setting	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] specify the address of the associated register. See the *Addressing Register* section for more details.	0x0	R/W
8	reserved		reserved.	0x0	R/W
[7:5]	V7B		V7B voltage range selection.	0x3	R/W
		00	V7B ± 10V.		
		01	V7B ± 2.5V.		
		10	V7B ±5V.		
		11	V7B ± 10V.		
[5:4]	V6B		V6B voltage range selection.	0x3	R/W

Bit	Bit Name	Setting	Description	Reset	Access
		00	V6B ± 10V.		
		01	V6B ± 2.5V.		
		10	V6B ±5V.		
		11	V6B ± 10V.		
[3:2]	V5B		V5B voltage range selection.	0x3	R/W
		00	V5B ± 10V.		
		01	V5B ± 2.5V.		
		10	V5B ±5V.		
		11	V5B ± 10V.		
[1:0]	V4B		V4B voltage range selection.	0x3	R/W
		00	V4B ± 10V.		
		01	V4B ± 2.5V.		
		10	V4B ±5V.		
		11	V4B ± 10V.		

12.5 Sequencer Stack Registers

Although the channel registers define the next channel to be converted (whether it is a diagnostic channel or a pair of analog input channels), if many analog input channels are to be sampled, it is convenient to utilize the 32 sequencer stack registers. In the communications register, when the REGADDR5 bit is set to logic 1, the contents of REGADDR [4:0] specify one of the 32 sequencer stack registers. In each sequencer stack register, the user can specify a pair of analog inputs to be sampled simultaneously.

The structure of the sequence forms a stack where each row represents two channels to be converted synchronously. The sequence starts at Sequencer Stack Register 1 and loops through Sequencer Stack Register 32. If Bit D8 (Enable Bit SSRENx) in one of the Sequencer Stack Registers is set to 1, the sequence ends at the analog input pair defined by that register and loops back to the first Sequencer Stack Register. By default, the Sequencer Stack Registers are set to loop through Channel V0A and Channel V0B to Channel V7A and Channel V7B. After a full or partial reset is initiated, the Sequencer Stack Registers are reinitialized and loop through Channel V0A and Channel V0B to Channel V7A and Channel V7B.

Address: 0x20 to 0x3F; Reset: 0x0000; Name: Sequencer Stack Register [0:31]

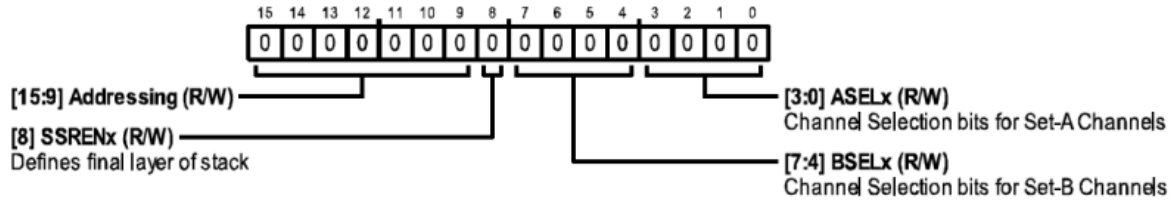


Table 19. Bit Description of Sequencer Stack Register [0:31]

Bit	Bit Name	Setting	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] specify the address of the associated register. See the *Addressing Register* section for more details.	0x0	R/W

Bit	Bit Name	Setting	Description	Reset	Access
8	SSREN[0:31]		When this bit is set to 0, it instructs the ADC to move to the next level of the sequencer stack after converting the current channel pair. When this bit is set to 1, it defines this level of the sequencer stack as the last level in the sequence. The sequencer then loops back to the first level of the stack.	0x0	R/W
[7:4]	BSEL[0:31]		Channel select bits for ADC B channel.		
		0000	V0B.		
		0001	V1B.		
		0010	V2B.		
		0011	V3B.		
		0100	V4B.		
		0101	V5B.		
		0110	V6B.		
		0111	V7B.		
		1000	VCC		
		1001	ALDO		
		1010	reserve.		
		1011	Set the dedicated bit for the digital interface communication self-test function. When reading the transition code, the code 0xAAAA is read out as the transition code of channel A, and the code 0x5555 is read out as the transition code of channel B.		
		1100	reserved.		
[3:0]	ASEL[0:31]		Channel select bit for ADC A channel. Same settings as ADC B.	0x0	R/W

1. After a full or partial reset is initiated, the sequencer stack registers are reinitialized, traversing from Channel V0A and Channel V0B to Channel V7A and Channel V7B and looping. The remaining 24 levels of the stack are reinitialized to 0x0.

12.6 Status Register

The status register is a 16-bit read-only register. If the STATUSEN bit in the configuration register is set to logic 1, the status register is read out at the end of all conversion words for the selected channel (including the self-test channel if enabled in sequencer mode).

MSB

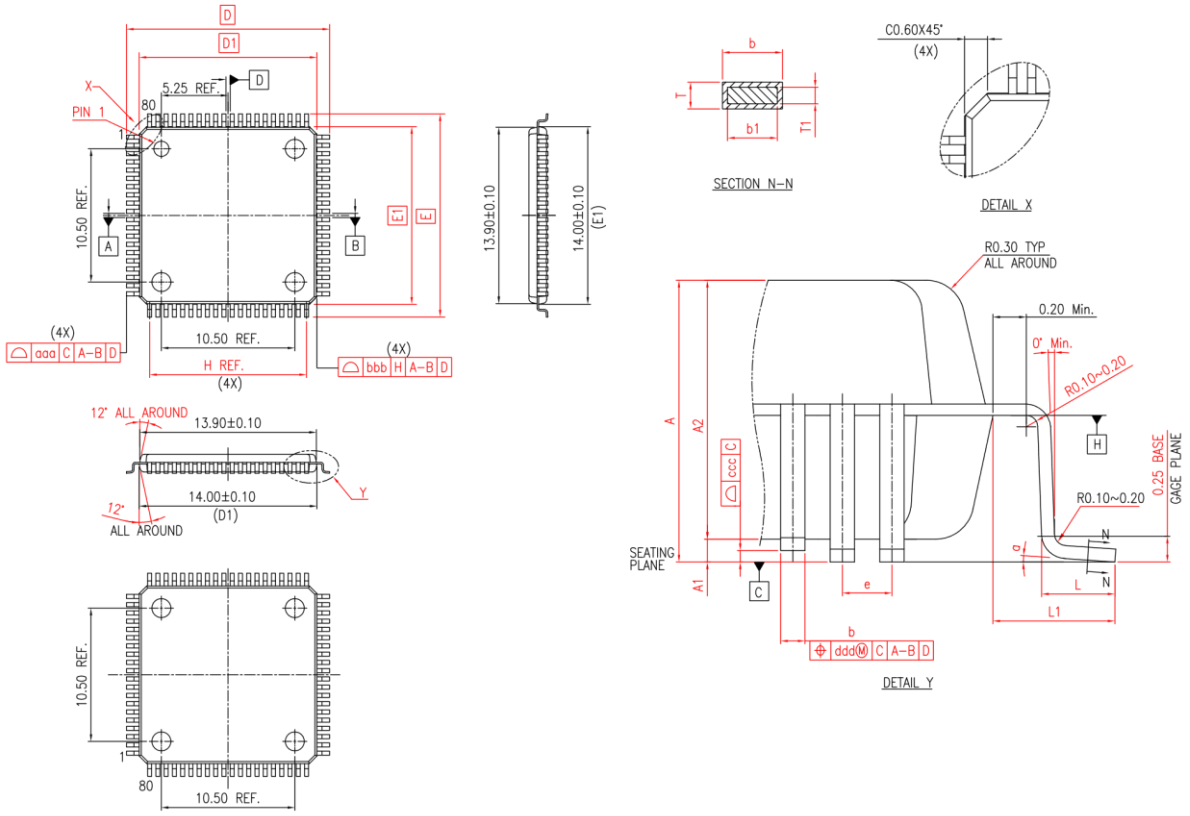
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A[3:0]				B[3:0]											

Table 20. Status Register Bit Description

Bit	Bit Name	setting	Description	Reset[1]	Access
[D15:D12]	A[3:0]		Channel index of the previous conversion result on channel A.	N/A	R
[D11:D8]	B[3:0]		Channel index of the previous conversion result on channel B.	N/A	R
[D7:D0]				N/A	R

1. N/A means not applicable.

13 Packaging Information



DIMENSION LIST (FOOTPRINT: 2.00)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.10±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	16.00±0.20	LEAD TIP TO TIP
5	D1	14.00±0.10	PKG LENGTH
6	E	16.00±0.20	LEAD TIP TO TIP
7	E1	14.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF.	LEAD LENGTH
10	T	$0.15^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.32±0.06	LEAD WIDTH
14	b1	0.30±0.03	LEAD BASE METAL WIDTH
15	e	0.65 BASE	LEAD PITCH
16	H(REF.)	(12.35)	CUM. LEAD PITCH
17	aaa	0.20	PROFILE OF LEAD TIPS
18	bbb	0.20	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.10
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXPECT EJECTION AND PIN 1 MARKING.		Ra0.8~2.0um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.20
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

14 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30AD33G0VWTR-I10	LQFP80	Green	Tape & Reel	1000	−40°C to +125°C

15 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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